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Introspect Technology

Interoperability Challenges and Solutions for MIPI I3C℠

MOBILE & BEYOND

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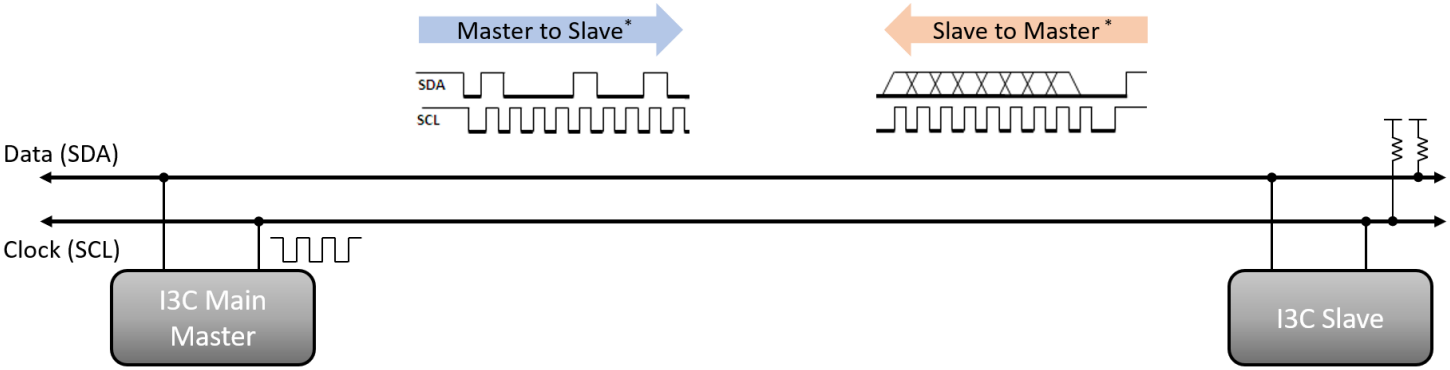
Interoperability Challenges and Solutions for MIPI I3C℠

- I3C: A Brief Overview
- Interoperability Challenges
  - Board layout and component optimization
  - Signal timing adjustment
  - Protocol implementation
- Conclusions and Best Practices

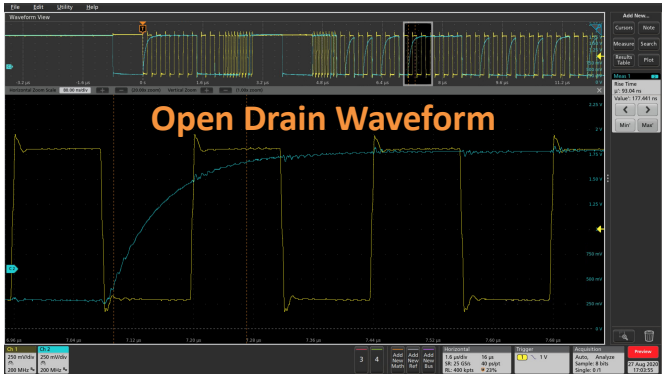
To begin… what is MIPI I3C℠?

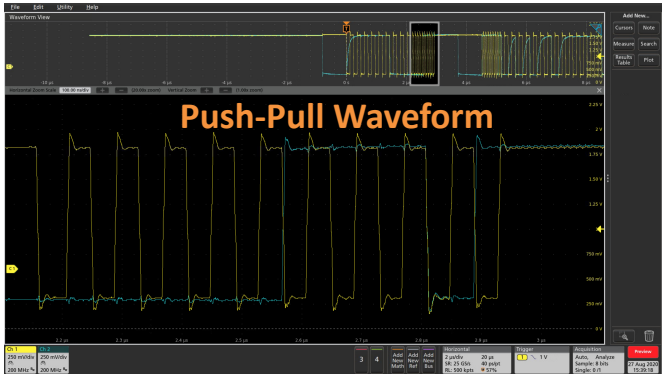


- What makes I3C so innovative?
  - I3C introduces higher bandwidth operating modes
  - I3C provides a very flexible system architecture
  - I3C has the potential to reduce pin counts on sensor interfaces

MIPI I3C℠ Data Rates

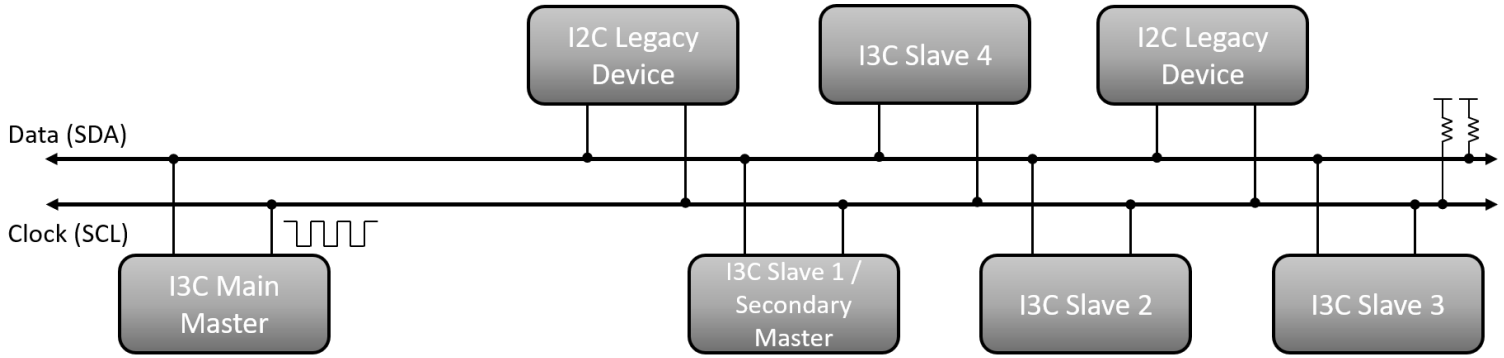
- Open Drain: up to 4.0 MHz
- Push Pull: up to 12.5 MHz
- HDR-DDR: up to 25 MHz
- HDR-Ternary: up to 33 MHz
- MIPI I3C v1.1 has new modes as well





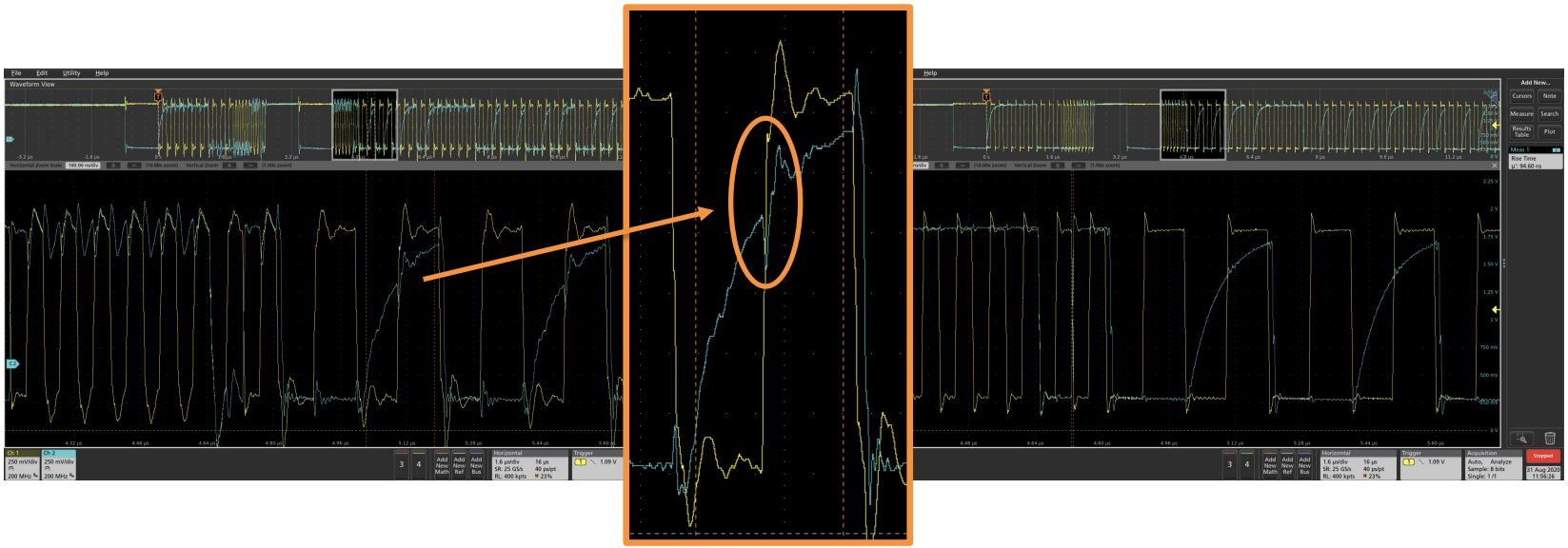
MIPI I3C℠: Interoperation

- The vision for the I3C is that it that it will be adopted within multiple sensor and controller applications
- I3C implemented by different manufacturers and industries, often with very different control and bandwidth requirements
- Legacy I2C devices can be placed on the bus too



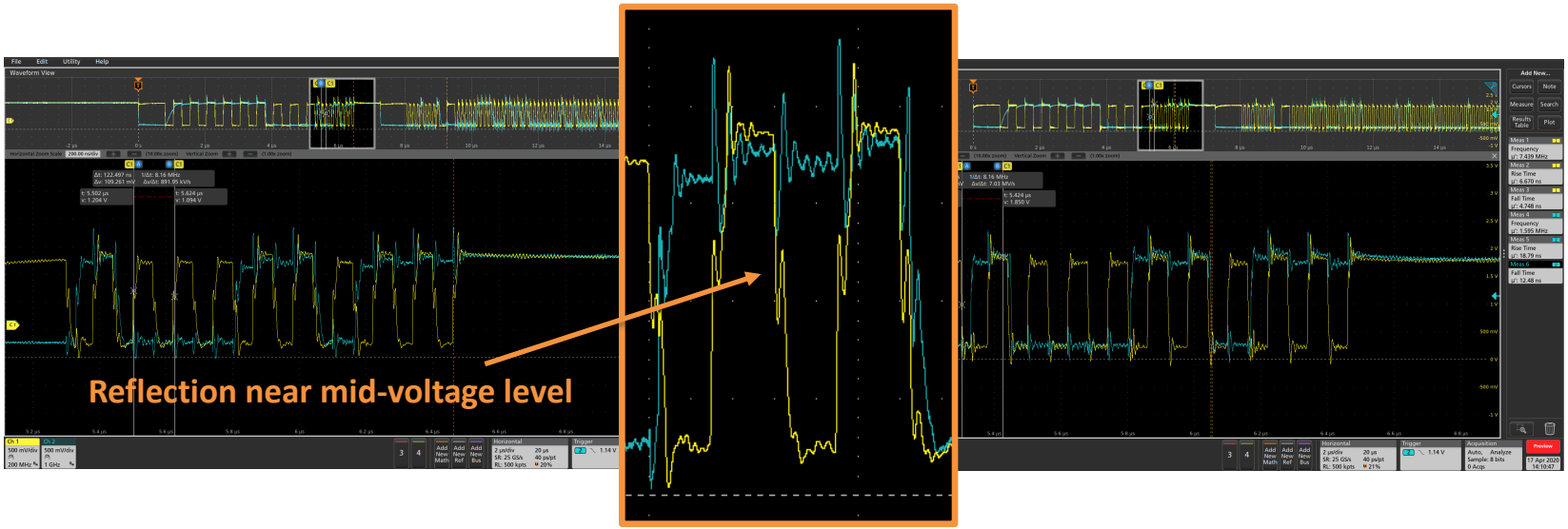
Board Design and Layout

- Some basic guidelines: attention to power and ground
  - On left: master and slave on separate ground planes, connected by wire
  - On right: master and slave on the same ground plane



Board Design and Layout

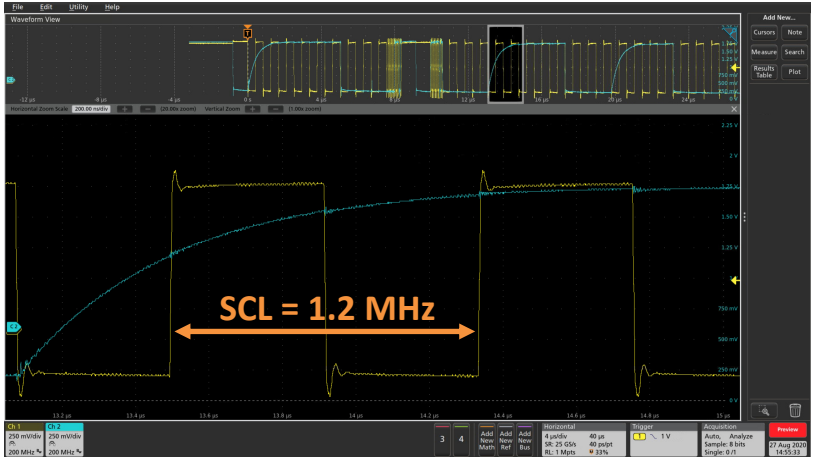
- Some basic guidelines: design boards with testing in mind
  - On left: 3 x 6 inch traces for 3 x I2C devices connected to bus
  - On right: with jumper removed, the 3 x 6 inch traces are removed from bus



Open Drain and Component Optimization

- Can you interoperate with a very capacitive bus?
  - Typically, use R = 2.83 kΩ for pull up resistors
  - This assumes rise time = 120 ns, line capacitance = 50 pF

- Problem: what if bus capacitance is as high as 180 pF!
- In this case, can only interoperate up to a data rate of 1.2 MHz



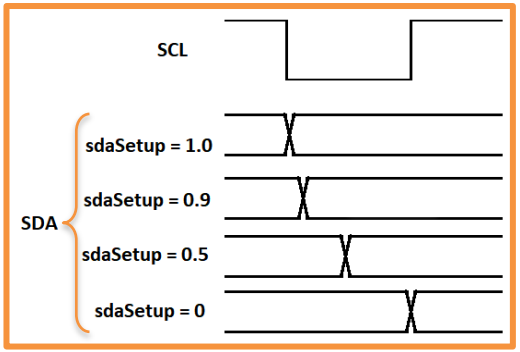
Open Drain and Component Optimization

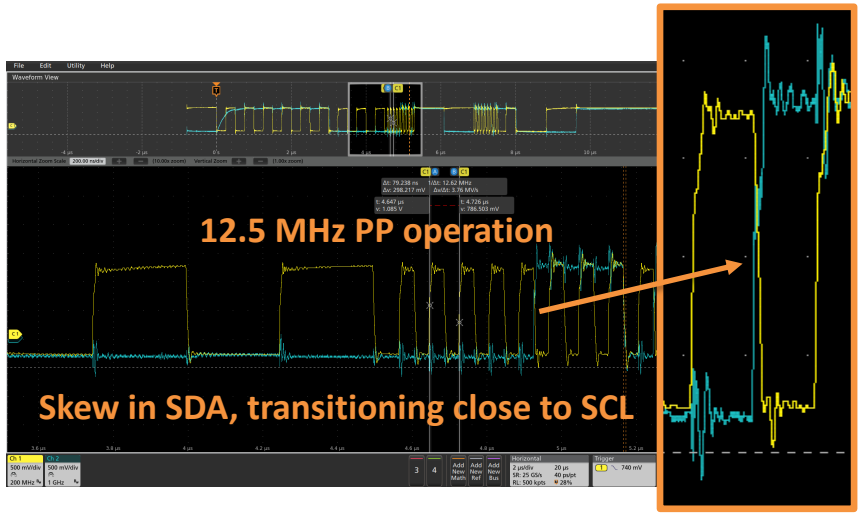
- Problem: how can the RC time constant be reduced to allow 4 MHz open drain operation?
- Solution: reduce the pull up resistance.
- Trade off: must keep V_{OD} < 270 mV. The design meets V_{OD} spec.

  - Note reflection on SDA from 24 inch trace, with no back termination. There is time for the reflection to settle.

Push-Pull and Timing Control

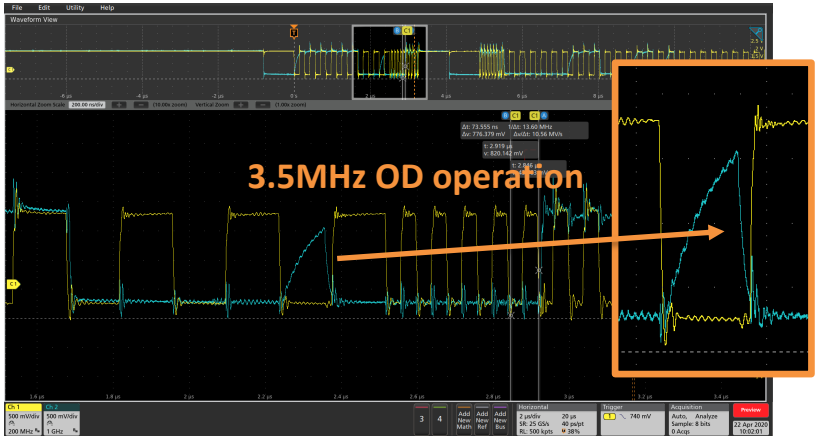
- On left, successful interoperation at 10 MHz push-pull
- On right, interoperation failures at 12.5 MHz push pull
- Problem: SCL/SDA skew as a function of data rate
- One solution: adjust the sampling control on the master





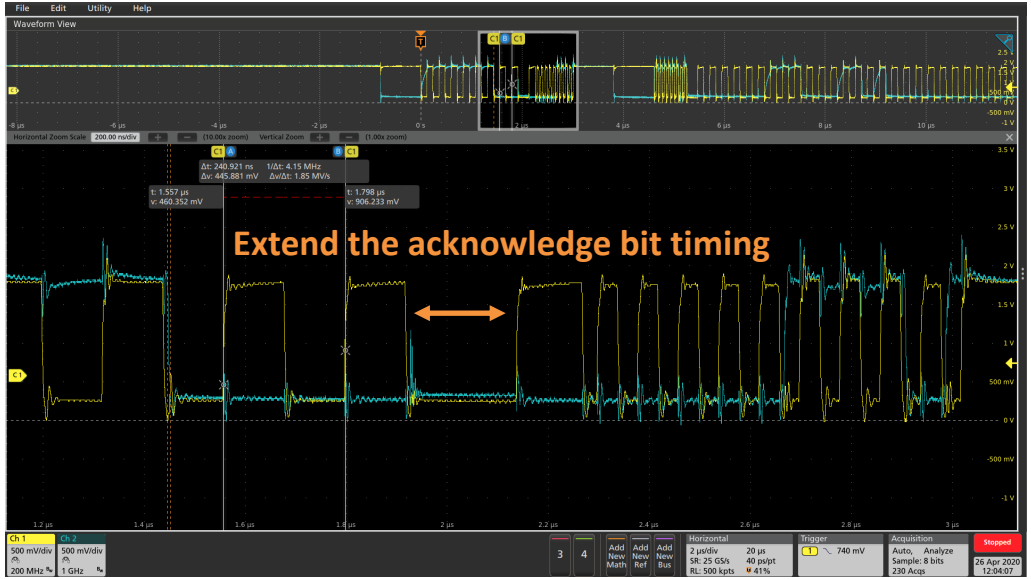
More on Timing Control

- On left: open drain = 3.5 MHz operation
- On right: open drain = 4.0 MHz operation
- Look at acknowledge bit. With this DUT, acknowledge was not instantaneous
- Result: Slave doesn't respond in time at 4.0 MHz



More on Timing Control

- One solution: master could delay the SCL edge during the acknowledge bit to provide additional time for slave to respond.



Protocol Implementation

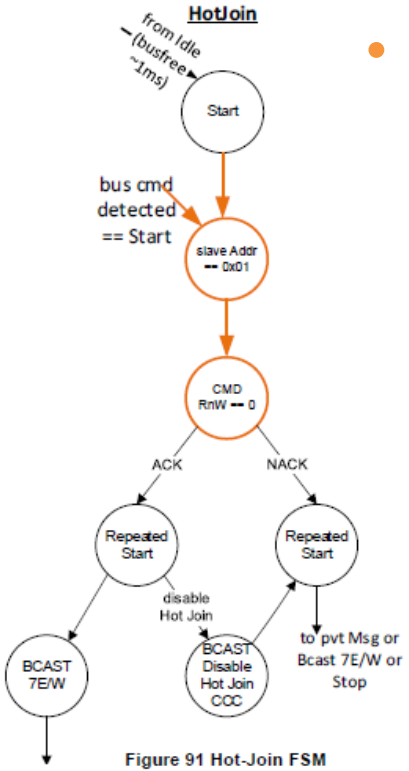


Figure 91 Hot-Join FSM

- Interoperation example: Hot Join

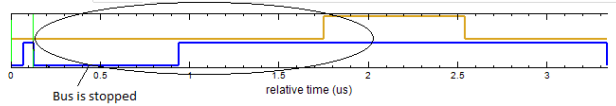
364 PHY States, 31 I3C States, 3 Messages

Go To: Timestamp... Times: relativeToStart FSM

PHY | I3C States | Messages

ID	Time (us)	Description	Param	PHY States	Duration (us)	Message
0	0.000	DELIM_BUS_IDLE	0x00	0-0 (1)	0.800	
1	0.800	SDR_BCAST_I3C_WR	0xFC	1-18 (18)	1.000	0
2	1.800	SDR_BCAST_I3C_ACK	0x00	19-20 (2)	0.125	
3	1.925	SDR_BCAST_CCC	0x00	21-36 (16)	0.430	
4	2.355	SDR_BCAST_CCC_TBIT	0x01	37-38 (2)	0.050	
5	2.405	SDR_BCAST_WR_DA...	0x08	39-55 (17)	0.425	
6	2.830	SDR_BCAST_WR_TBIT	0x00	56-57 (2)	0.050	
7	2.880	DELIM_BUS_IDLE	0x00	58-61 (4)	15482.625	
8	15485.505	HJ_ADDR	0x04	62-79 (18)	1.000	1
9	15486.505	HJ_ADDR_ACK	0x00	80-81 (2)	0.125	
10	15486.630	DELIM_BUS_IDLE	0x00	82-85 (4)	3.210	
11	15489.840	SDR_BCAST_I3C_WR	0xFC	86-103 (18)	1.000	2
12	15490.840	SDR_BCAST_I3C_ACK	0x00	104-105 (2)	0.125	
13	15490.965	SDR_BCAST_CCC	0x07	106-121 (16)	0.425	
14	15491.390	SDR_BCAST_CCC_TBIT	0x00	122-123 (2)	0.055	

PHY States 80-85



Protocol Implementation

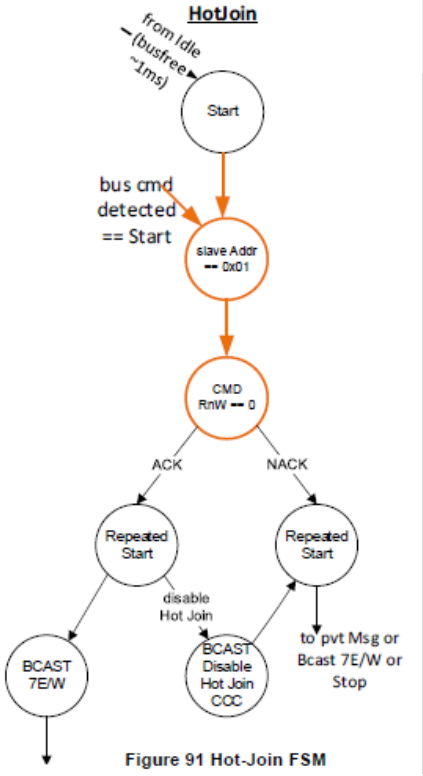


Figure 91 Hot-Join FSM

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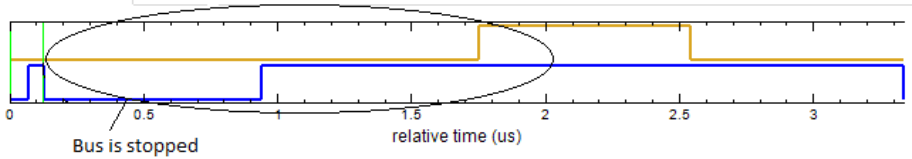
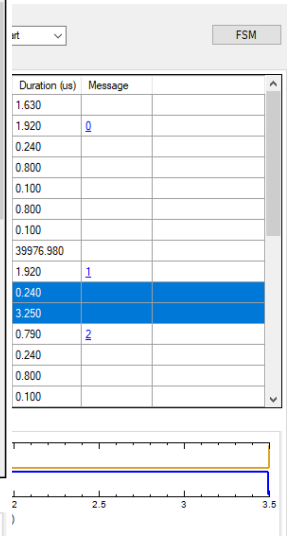
1	0.800	SDR_BCAST_I3C_WR	0xFC	1-18 (18)	1.000	0
2	1.800	SDR_BCAST_I3C_ACK	0x00	19-20 (2)	0.125	
3	1.925	SDR_BCAST_CCC	0x00	21-36 (16)	0.430	
4	2.355	SDR_BCAST_CCC_TBIT	0x01	37-38 (2)	0.050	
5	2.405	SDR_BCAST_WR_DA...	0x08	39-55 (17)	0.425	
6	2.830	SDR_BCAST_WR_TBIT	0x00	56-57 (2)	0.050	
7	2.880	DELIM_BUS_IDLE	0x00	58-61 (4)	15482.625	
8	15485.505	HJ_ADDR	0x04	62-79 (18)	1.000	1
9	15486.505	HJ_ADDR_ACK	0x00	80-81 (2)	0.125	
10	15486.630	DELIM_BUS_IDLE	0x00	82-85 (4)	3.210	
11	15489.840	SDR_BCAST_I3C_WR	0xFC	86-103 (18)	1.000	2
12	15490.840	SDR_BCAST_I3C_ACK	0x00	104-105 (2)	0.125	
13	15490.965	SDR_BCAST_CCC	0x07	106-121 (16)	0.425	
14	15491.390	SDR_BCAST_CCC_TBIT	0x00	122-123 (2)	0.055	

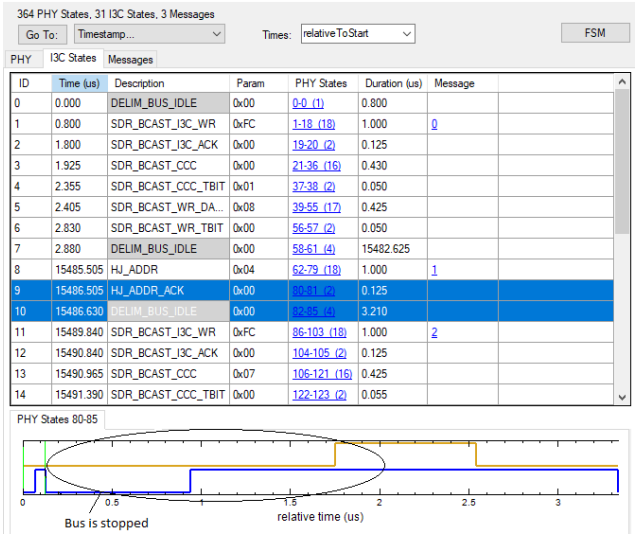
PHY States 80-85

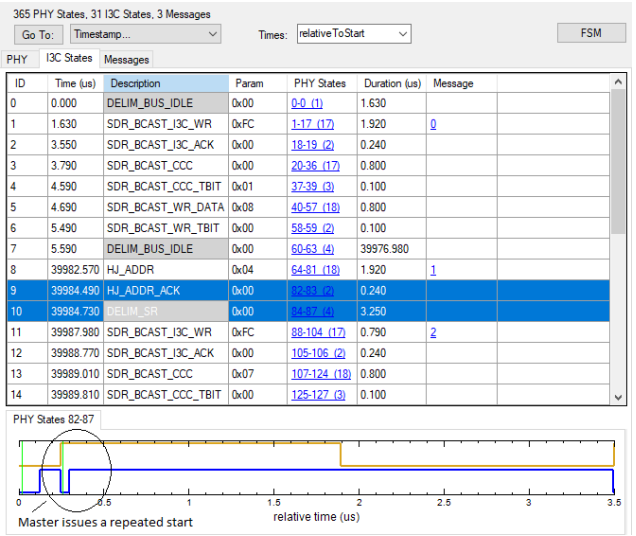




Protocol Implementation

- Interoperation example: Hot Join





- On left: after the slave's HJ request has been acknowledged, bus goes idle.
- On right: after the slave's HJ request has been acknowledged, the master issues a repeated start

Protocol Implementation

HotJoin

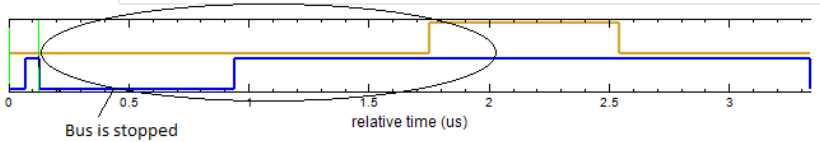
364 PHY States, 31 I3C States, 3 Messages

Go To: Timestamp... Times: relativeToStart FSM

PHY | I3C States | Messages

ID	Time (us)	Description	Param	PHY States	Duration (us)	Message
0	0.000	DELIM_BUS_IDLE	0x00	0-0 (1)	0.800	
1	0.800	SDR_BCAST_I3C_WR	0xFC	1-18 (18)	1.000	0
2	1.800	SDR_BCAST_I3C_ACK	0x00	19-20 (2)	0.125	
3	1.925	SDR_BCAST_CCC	0x00	21-36 (16)	0.430	
4	2.355	SDR_BCAST_CCC_TBIT	0x01	37-38 (2)	0.050	
5	2.405	SDR_BCAST_WR_DA...	0x08	39-55 (17)	0.425	
6	2.830	SDR_BCAST_WR_TBIT	0x00	56-57 (2)	0.050	
7	2.880	DELIM_BUS_IDLE	0x00	58-61 (4)	15482.625	
8	15485.505	HJ_ADDR	0x04	62-79 (18)	1.000	1
9	15486.505	HJ_ADDR_ACK	0x00	80-81 (2)	0.125	
10	15486.630	DELIM_BUS_IDLE	0x00	82-85 (4)	3.210	
11	15489.840	SDR_BCAST_I3C_WR	0xFC	86-103 (18)	1.000	2
12	15490.840	SDR_BCAST_I3C_ACK	0x00	104-105 (2)	0.125	
13	15490.965	SDR_BCAST_CCC	0x07	106-121 (16)	0.425	
14	15491.390	SDR_BCAST_CCC_TBIT	0x00	122-123 (2)	0.055	

PHY States 80-85



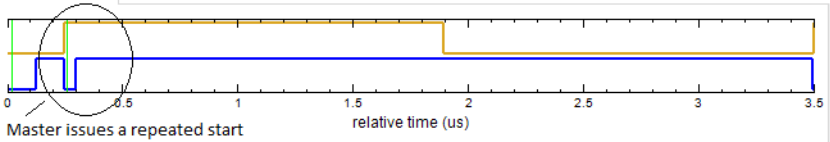
365 PHY States, 31 I3C States, 3 Messages

Go To: Timestamp... Times: relativeToStart FSM

PHY | I3C States | Messages

ID	Time (us)	Description	Param	PHY States	Duration (us)	Message
0	0.000	DELIM_BUS_IDLE	0x00	0-0 (1)	1.630	
1	1.630	SDR_BCAST_I3C_WR	0xFC	1-17 (17)	1.920	0
2	3.550	SDR_BCAST_I3C_ACK	0x00	18-19 (2)	0.240	
3	3.790	SDR_BCAST_CCC	0x00	20-36 (17)	0.800	
4	4.590	SDR_BCAST_CCC_TBIT	0x01	37-39 (3)	0.100	
5	4.690	SDR_BCAST_WR_DATA	0x08	40-57 (18)	0.800	
6	5.490	SDR_BCAST_WR_TBIT	0x00	58-59 (2)	0.100	
7	5.590	DELIM_BUS_IDLE	0x00	60-63 (4)	39976.980	
8	39982.570	HJ_ADDR	0x04	64-81 (18)	1.920	1
9	39984.490	HJ_ADDR_ACK	0x00	82-83 (2)	0.240	
10	39984.730	DELIM_SR	0x00	84-87 (4)	3.250	
11	39987.980	SDR_BCAST_I3C_WR	0xFC	88-104 (17)	0.790	2
12	39988.770	SDR_BCAST_I3C_ACK	0x00	105-106 (2)	0.240	
13	39989.010	SDR_BCAST_CCC	0x07	107-124 (18)	0.800	
14	39989.810	SDR_BCAST_CCC_TBIT	0x00	125-127 (3)	0.100	

PHY States 82-87



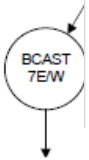
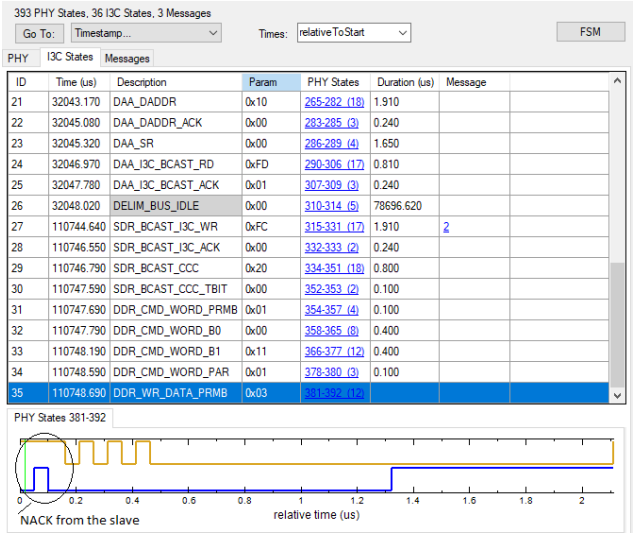


Figure 91 Hot-Join FSM

- On right: after the slave's HJ request has been acknowledged, the master issues a repeated start

Protocol Implementation

- Interoperation example: HDR-DDR



Protocol Implementation

- Interoperat

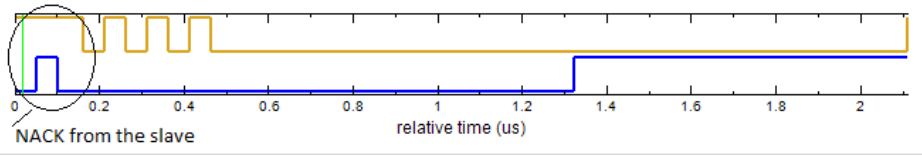
393 PHY States, 36 I3C States, 3 Messages

Go To: Timestamp... Times: relativeToStart FSM

PHY | I3C States | Messages

ID	Time (us)	Description	Param	PHY States	Duration (us)	Message
21	32043.170	DAA_DADDR	0x10	265-282 (18)	1.910	
22	32045.080	DAA_DADDR_ACK	0x00	283-285 (3)	0.240	
23	32045.320	DAA_SR	0x00	286-289 (4)	1.650	
24	32046.970	DAA_I3C_BCAST_RD	0xFD	290-306 (17)	0.810	
25	32047.780	DAA_I3C_BCAST_ACK	0x01	307-309 (3)	0.240	
26	32048.020	DELIM_BUS_IDLE	0x00	310-314 (5)	78696.620	
27	110744.640	SDR_BCAST_I3C_WR	0xFC	315-331 (17)	1.910	2
28	110746.550	SDR_BCAST_I3C_ACK	0x00	332-333 (2)	0.240	
29	110746.790	SDR_BCAST_CCC	0x20	334-351 (18)	0.800	
30	110747.590	SDR_BCAST_CCC_TBIT	0x00	352-353 (2)	0.100	
31	110747.690	DDR_CMD_WORD_PRMB	0x01	354-357 (4)	0.100	
32	110747.790	DDR_CMD_WORD_B0	0x00	358-365 (8)	0.400	
33	110748.190	DDR_CMD_WORD_B1	0x11	366-377 (12)	0.400	
34	110748.590	DDR_CMD_WORD_PAR	0x01	378-380 (3)	0.100	
35	110748.690	DDR_WR_DATA_PRMB	0x03	381-392 (12)		

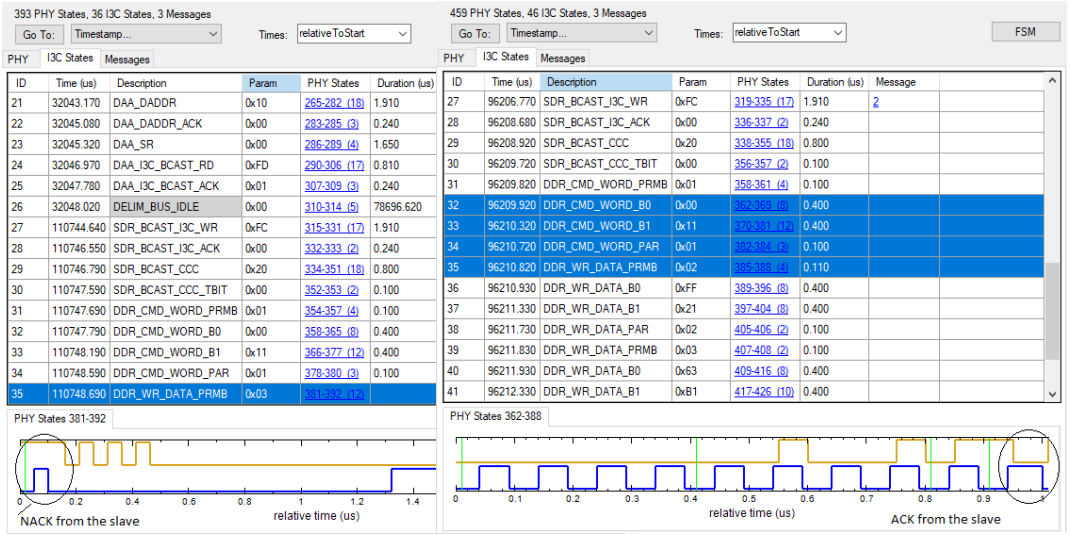
PHY States 381-392



  - Unsuccessfu
  - Underlying i

Protocol Implementation

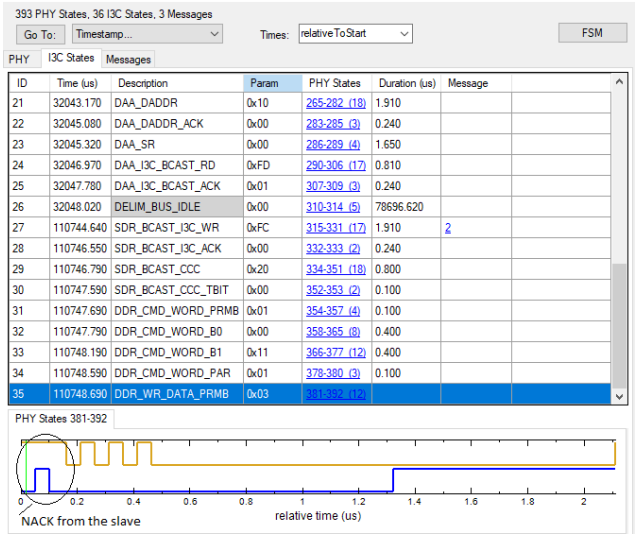
- Interoperation example: HDR-DDR

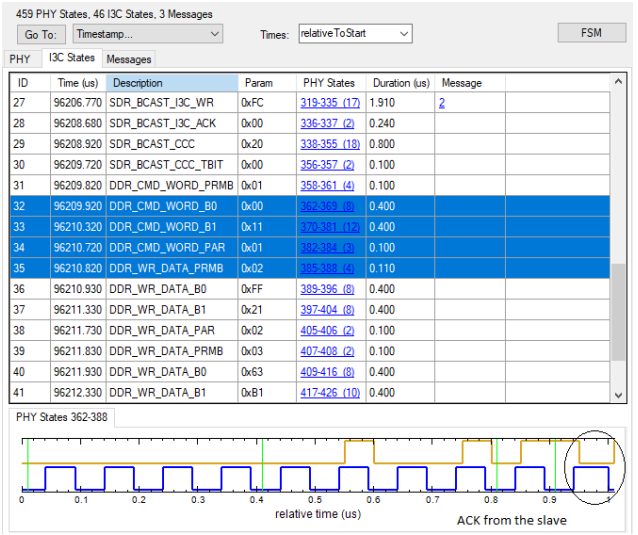


  - On left: unsuccessful DDR write: the slave issues a NACK
  - On right: successful DDR write: the master receives an ACK from slave

Protocol Implementation

- Interoperation example: HDR-DDR





  - On left: unsuccessful DDR write: the slave issues a NACK
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Protocol Implementation

Interoperation example: HDR-DDR

393 PHY States, 36 I2C States, 3 Messages

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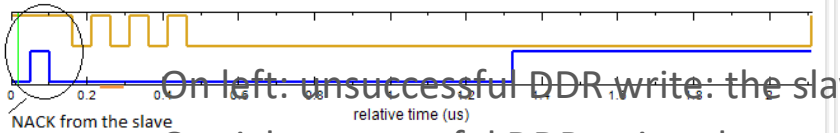
22	32045.080	DAA_DADDR_ACK	0x00	283-285 (3)	0.240	
23	32045.320	DAA_SR	0x00	286-289 (4)	1.650	
24	32046.970	DAA_I3C_BCAST_RD	0xFD	290-306 (17)	0.810	
25	32047.780	DAA_I3C_BCAST_ACK	0x01	307-309 (3)	0.240	
26	32048.020	DELIM_BUS_IDLE	0x00	310-314 (5)	78696.620	
27	110744.640	SDR_BCAST_I3C_WR	0xFC	315-331 (17)	1.910	2
28	110746.550	SDR_BCAST_I3C_ACK	0x00	332-333 (2)	0.240	
29	110746.790	SDR_BCAST_CCC	0x20	334-351 (18)	0.800	
30	110747.590	SDR_BCAST_CCC_TBIT	0x00	352-353 (2)	0.100	
31	110747.690	DDR_CMD_WORD_PRMB	0x01	354-357 (4)	0.100	
32	110747.790	DDR_CMD_WORD_B0	0x00	358-365 (8)	0.400	
33	110748.190	DDR_CMD_WORD_B1	0x11	366-377 (12)	0.400	
34	110748.590	DDR_CMD_WORD_PAR	0x01	378-380 (3)	0.100	
35	110748.690	DDR_WR_DATA_PRMB	0x03	381-392 (12)		

PHY States 381-392



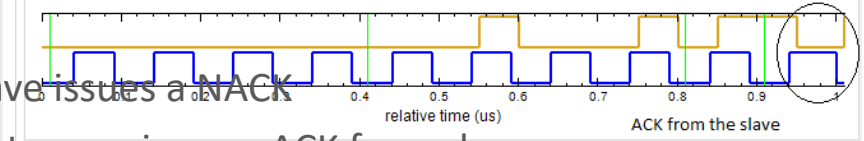
459 PHY States, 46 I3C States, 3 Messages

Go To: Timestamp... Times: relativeToStart FSM

PHY | I3C States | Messages

ID	Time (us)	Description	Param	PHY States	Duration (us)	Message
27	96206.770	SDR_BCAST_I3C_WR	0xFC	319-335 (17)	1.910	2
28	96208.680	SDR_BCAST_I3C_ACK	0x00	336-337 (2)	0.240	
29	96208.920	SDR_BCAST_CCC	0x20	338-355 (18)	0.800	
30	96209.720	SDR_BCAST_CCC_TBIT	0x00	356-357 (2)	0.100	
31	96209.820	DDR_CMD_WORD_PRMB	0x01	358-361 (4)	0.100	
32	96209.920	DDR_CMD_WORD_B0	0x00	362-369 (8)	0.400	
33	96210.320	DDR_CMD_WORD_B1	0x11	370-381 (12)	0.400	
34	96210.720	DDR_CMD_WORD_PAR	0x01	382-384 (3)	0.100	
35	96210.820	DDR_WR_DATA_PRMB	0x02	385-388 (4)	0.110	
36	96210.930	DDR_WR_DATA_B0	0xFF	389-396 (8)	0.400	
37	96211.330	DDR_WR_DATA_B1	0x21	397-404 (8)	0.400	
38	96211.730	DDR_WR_DATA_PAR	0x02	405-406 (2)	0.100	
39	96211.830	DDR_WR_DATA_PRMB	0x03	407-408 (2)	0.100	
40	96211.930	DDR_WR_DATA_B0	0x63	409-416 (8)	0.400	
41	96212.330	DDR_WR_DATA_B1	0xB1	417-426 (10)	0.400	

PHY States 362-388



- On left: unsuccessful DDR write: the slave issues a NACK
- On right: successful DDR write: the master receives an ACK from slave
- **Analyzer tools ensure interoperation debug goes smoothly**

Conclusions and Best Practices

- MIPI® I3C℠ has great potential to provide a fast sensor and control bus, and can save a lot of pins on devices and traces on PCBs
- To help ensure interoperability:
  - First principles for layout
    - Power and ground, designing buses for test, bus capacitance
  - Understand signal timing issues
    - Small adjustments can make a big difference for interoperability
  - Protocol implementation
    - Having analysis tools can help make interoperability debug smooth

ADDITIONAL RESOURCES

- https://www.mipi.org/specifications/i3c-sensor-specification
  - MIPI® I3C℠ Specifications
- https://www.mipi.org/sites/default/files/mipi_I3C-and-I3C-Basic_app-note-system-integrator
  - System Integrators Application Note for MIPI® I3C℠ v1.0 and I3C℠ Basic v1.0
- https://introspect.ca/
  - Total solutions for most high-speed interface technologies
- https://introspect.ca/products-solutions/i3c-design-and-test/
  - I3C design and test solutions
- https://register.gotowebinar.com/register/8766219688391017985
  - I3C Webinar

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