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Interoperability Challenges and Solutions for MIPI I3C[™]

MOBILE & BEYOND

MIPI ALLIANCE DEVELOPERS CONFERENCE

22-23 SEPTEMBER 2020

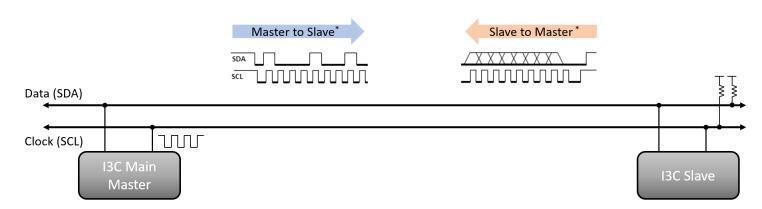
Interoperability Challenges and Solutions for MIPI I3C[™]

- I3C: A Brief Overview
- Interoperability Challenges
 - Board layout and component optimization
 - Signal timing adjustment
 - Protocol implementation
- Conclusions and Best Practices

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To begin... what is MIPI I3C[™]?



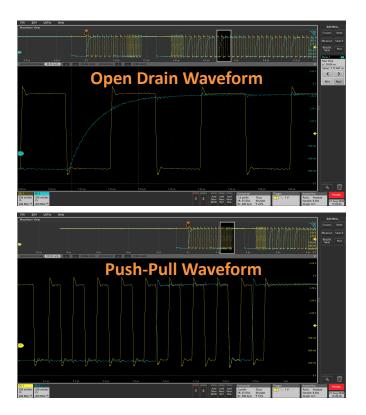
- What makes I3C so innovative?
 - I3C introduces higher bandwidth operating modes
 - I3C provides a very flexible system architecture
 - I3C has the potential to reduce pin counts on sensor interfaces

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MIPI I3C[™] Data Rates

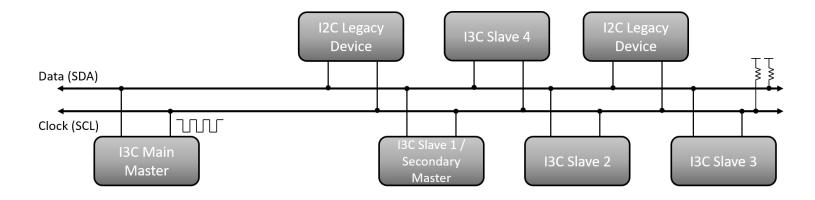
- Open Drain: up to 4.0 MHz
- Push Pull: up to 12.5 MHz
- HDR-DDR: up to 25 MHz
- HDR-Ternary: up to 33 MHz
- MIPI I3C v1.1 has new modes as well





MIPI I3CsM: Interoperation

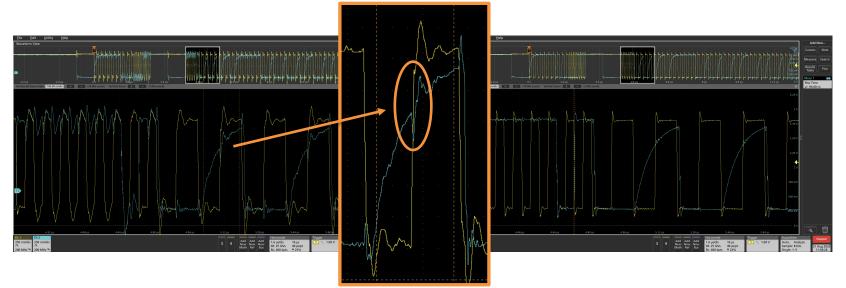
- The vision for the I3C is that it that it will be adopted within multiple sensor and controller applications
- I3C implemented by different manufacturers and industries, often with very different control and bandwidth requirements
- Legacy I2C devices can be placed on the bus too





Board Design and Layout

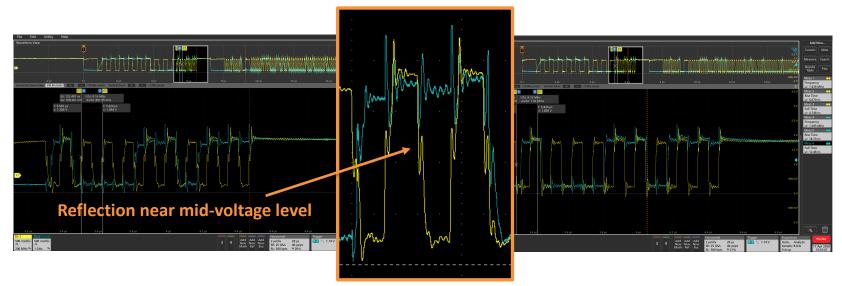
- Some basic guidelines: attention to power and ground
 - On left: master and slave on separate ground planes, connected by wire
 - On right: master and slave on the same ground plane





Board Design and Layout

- Some basic guidelines: design boards with testing in mind
 - On left: 3 x 6 inch traces for 3 x I2C devices connected to bus
 - On right: with jumper removed, the 3 x 6 inch traces are removed from bus





Open Drain and Component Optimization

- Can you interoperate with a very capacitive bus?
 - Typically, use R = 2.83 k Ω for pull up resistors
 - This assumes rise time = 120 ns, line capacitance = 50 pF
- Problem: what if bus capacitance is as high as 180 pF!
- In this case, can only interoperate up to a data rate of 1.2 MHz





Open Drain and Component Optimization

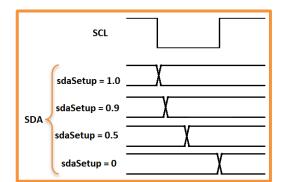
- Problem: how can the RC time constant be reduced to allow 4 MHz open drain operation?
- Solution: reduce the pull up resistance.
- Trade off: must keep V_{OD} < 270 mV. The design meets V_{OD} spec.
 - Note reflection on SDA from 24 inch trace, with no back termination. There is time for the reflection to settle.



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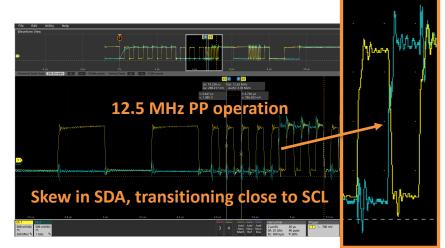
Push-Pull and Timing Control

- On left, successful interoperation at 10 MHz push-pull
- On right, interoperation failures at 12.5 MHz push pull
- Problem: SCL/SDA skew as a function of data rate
- One solution: adjust the sampling control on the master



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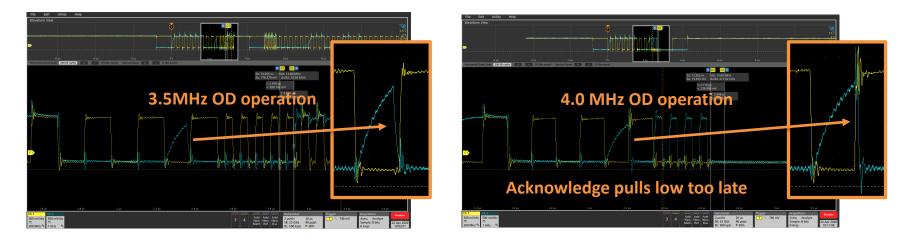






More on Timing Control

- On left: open drain = 3.5 MHz operation
- On right: open drain = 4.0 MHz operation
- Look at acknowledge bit. With this DUT, acknowledge was not instantaneous
- Result: Slave doesn't respond in time at 4.0 MHz



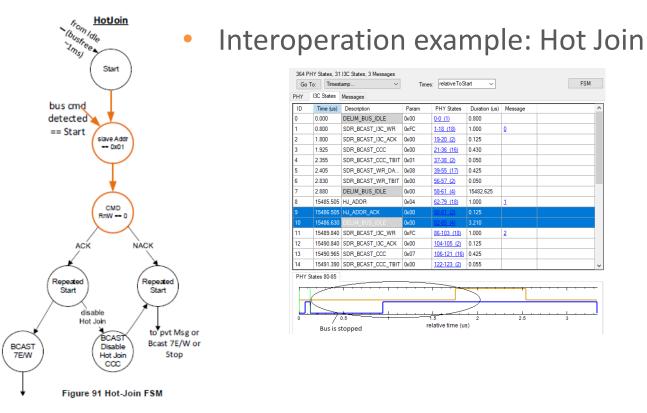


More on Timing Control

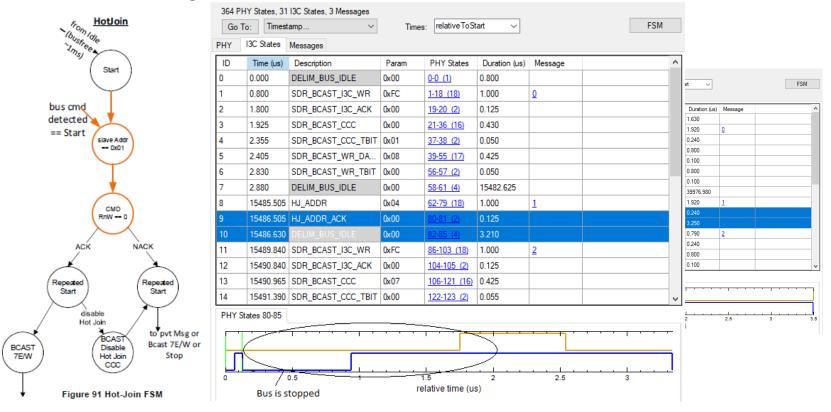
• One solution: master could delay the SCL edge during the acknowledge bit to provide additional time for slave to respond.













• Interoperation example: Hot Join

| ID | Time (us) | Description | Param | PHY States | Duration (us) | Message | ^ |
|----|-----------|--------------------|-------|---------------------|---------------|---------|---|
| 0 | 0.000 | DELIM BUS IDLE | 0x00 | 0-0 (1) | 0.800 | | |
| 1 | 0.800 | SDR_BCAST_I3C_WR | 0xFC | 1-18 (18) | 1.000 | 0 | |
| 2 | 1.800 | SDR_BCAST_I3C_ACK | 0x00 | 19-20 (2) | 0.125 | | |
| 3 | 1.925 | SDR_BCAST_CCC | 0x00 | 21-36 (16) | 0.430 | | |
| 4 | 2.355 | SDR_BCAST_CCC_TBIT | 0x01 | 37-38 (2) | 0.050 | | |
| 5 | 2.405 | SDR_BCAST_WR_DA | 0x08 | 39-55 (17) | 0.425 | | |
| 6 | 2.830 | SDR_BCAST_WR_TBIT | 0x00 | <u>56-57 (2)</u> | 0.050 | | |
| 7 | 2.880 | DELIM_BUS_IDLE | 0x00 | <u>58-61 (4)</u> | 15482.625 | | |
| 8 | 15485.505 | HJ_ADDR | 0x04 | <u>62-79 (18)</u> | 1.000 | 1 | |
| 9 | 15486.505 | HJ_ADDR_ACK | 0x00 | <u>80-81 (2)</u> | 0.125 | | |
| 10 | 15486.630 | DELIM_BUS_IDLE | 0x00 | <u>82-85 (4)</u> | 3.210 | | |
| 11 | 15489.840 | SDR_BCAST_I3C_WR | 0xFC | 86-103 (18) | 1.000 | 2 | |
| 12 | 15490.840 | SDR_BCAST_I3C_ACK | 0x00 | <u>104-105 (2)</u> | 0.125 | | |
| 13 | 15490.965 | SDR_BCAST_CCC | 0x07 | <u>106-121 (16)</u> | 0.425 | | |
| 14 | 15491.390 | SDR_BCAST_CCC_TBIT | 0x00 | 122-123 (2) | 0.055 | | ~ |

| Go | To: Timest | amp V | Times: | relativeToSta | art 🗸 | | | FSM |
|----------|--------------|--------------------|--------|--------------------|---------------|----------|---|-----|
| ΉY | I3C States | Messages | | | | | | |
| ID | Time (us) | Description | Param | PHY States | Duration (us) | Message | | |
| 0 | 0.000 | DELIM_BUS_IDLE | 0x00 | <u>0-0 (1)</u> | 1.630 | | | |
| 1 | 1.630 | SDR_BCAST_I3C_WR | 0xFC | <u>1-17 (17)</u> | 1.920 | <u>0</u> | | |
| 2 | 3.550 | SDR_BCAST_I3C_ACK | 0×00 | <u>18-19 (2)</u> | 0.240 | | | |
| 3 | 3.790 | SDR_BCAST_CCC | 0×00 | 20-36 (17) | 0.800 | | | |
| 4 | 4.590 | SDR_BCAST_CCC_TBIT | 0x01 | <u>37-39 (3)</u> | 0.100 | | | |
| 5 | 4.690 | SDR_BCAST_WR_DATA | 0×08 | 40-57 (18) | 0.800 | | | |
| 6 | 5.490 | SDR_BCAST_WR_TBIT | 0x00 | <u>58-59 (2)</u> | 0.100 | | | |
| 7 | 5.590 | DELIM_BUS_IDLE | 0×00 | <u>60-63 (4)</u> | 39976.980 | | | |
| 8 | 39982.570 | HJ_ADDR | 0x04 | 64-81 (18) | 1.920 | 1 | | |
| 9 | 39984.490 | HJ_ADDR_ACK | 0×00 | <u>82-83 (2)</u> | 0.240 | | | |
| 10 | 39984.730 | DELIM_SR | 0×00 | <u>84-87 (4)</u> | 3.250 | | | |
| 11 | 39987.980 | SDR_BCAST_I3C_WR | 0xFC | <u>88-104 (17)</u> | 0.790 | 2 | | |
| 12 | 39988.770 | SDR_BCAST_I3C_ACK | 0x00 | <u>105-106 (2)</u> | 0.240 | | | |
| 13 | 39989.010 | SDR_BCAST_CCC | 0x07 | 107-124 (18) | 0.800 | | | |
| 14 | 39989.810 | SDR_BCAST_CCC_TBIT | 0×00 | <u>125-127 (3)</u> | 0.100 | | | |
| PHY ! | States 82-87 | | | | | | | |
| | | | | | | | | |
| 1 | / | \ | | | | | | |
| | fi— | } | | | | | | |
| <u> </u> | | <u> </u> | 1.5 | | | 2.5 | 3 | |

- On left: after the slave's HJ request has been acknowledged, bus goes idle.
- On right: after the slave's HJ request has been acknowledged, the master issues a repeated start



| Go To | : Timest | amp V | Times | relativeToS | art 🗸 | | | FSM | G | To: Times | tamp V | limes | : relative To St | art 🗸 | | F3 | SM |
|----------|------------|--------------------|-------|----------------------|---------------|-----------------|----------|-------|-----|--------------|---------------------------|-------|---------------------|---------------|----------|----------|----|
| PHY | 3C States | Messages | | | | | | | PHY | I3C States | Messages | | | | | | |
| ID | Time (us) | Description | Param | PHY States | Duration (us) | Message | | ^ | ID | Time (us) | Description | Param | PHY States | Duration (us) | Message | | |
| 0 | 0.000 | DELIM_BUS_IDLE | 0x00 | <u>0-0 (1)</u> | 0.800 | | | | 0 | 0.000 | DELIM_BUS_IDLE | 0x00 | <u>0-0 (1)</u> | 1.630 | | | |
| 1 | 0.800 | SDR_BCAST_I3C_WR | 0xFC | <u>1-18 (18)</u> | 1.000 | <u>0</u> | | | 1 | 1.630 | SDR_BCAST_I3C_WR | 0xFC | <u>1-17 (17)</u> | 1.920 | <u>0</u> | | |
| 2 | 1.800 | SDR_BCAST_I3C_ACK | 0x00 | <u>19-20 (2)</u> | 0.125 | | | | 2 | 3.550 | SDR_BCAST_I3C_ACK | 0x00 | <u>18-19 (2)</u> | 0.240 | | | |
| 3 | 1.925 | SDR_BCAST_CCC | 0x00 | <u>21-36 (16)</u> | 0.430 | | | | 3 | 3.790 | SDR_BCAST_CCC | 0x00 | <u>20-36 (17)</u> | 0.800 | | | |
| 4 | 2.355 | SDR_BCAST_CCC_TBIT | 0x01 | <u>37-38 (2)</u> | 0.050 | | | | 4 | 4.590 | SDR_BCAST_CCC_TBIT | 0x01 | <u>37-39 (3)</u> | 0.100 | | | |
| 5 | 2.405 | SDR_BCAST_WR_DA | 0x08 | <u>39-55 (17)</u> | 0.425 | | | | 5 | 4.690 | SDR_BCAST_WR_DATA | 0x08 | <u>40-57 (18)</u> | 0.800 | | | |
| 6 | 2.830 | SDR_BCAST_WR_TBIT | 0x00 | <u>56-57 (2)</u> | 0.050 | | | | 6 | 5.490 | SDR_BCAST_WR_TBIT | 0x00 | <u>58-59 (2)</u> | 0.100 | | | |
| 7 | 2.880 | DELIM_BUS_IDLE | 0x00 | <u>58-61 (4)</u> | 15482.625 | | | | 7 | 5.590 | DELIM_BUS_IDLE | 0x00 | <u>60-63 (4)</u> | 39976.980 | | | |
| 8 | 15485.505 | HJ_ADDR | 0x04 | <u>62-79 (18)</u> | 1.000 | 1 | | | 8 | 39982.570 | HJ_ADDR | 0x04 | <u>64-81 (18)</u> | 1.920 | 1 | | |
| 9 | 15486.505 | HJ_ADDR_ACK | 0x00 | <u>80-81 (2)</u> | 0.125 | | | | 9 | 39984.490 | HJ_ADDR_ACK | 0x00 | <u>82-83 (2)</u> | 0.240 | | | |
| 10 | 15486.630 | DELIM_BUS_IDLE | 0x00 | 82-85 (4) | 3.210 | | | | 10 | 39984.730 | DELIM_SR | 0x00 | 84-87 (4) | 3.250 | | | |
| 11 | 15489.840 | SDR_BCAST_I3C_WR | 0xFC | <u>86-103 (18)</u> | 1.000 | 2 | | | 11 | 39987.980 | SDR_BCAST_I3C_WR | 0xFC | <u>88-104 (17)</u> | 0.790 | 2 | | |
| 12 | 15490.840 | SDR_BCAST_I3C_ACK | 0x00 | <u>104-105 (2)</u> | 0.125 | | | | 12 | 39988.770 | SDR_BCAST_I3C_ACK | 0x00 | <u>105-106 (2)</u> | 0.240 | | | |
| 13 | 15490.965 | SDR_BCAST_CCC | 0x07 | <u>106-121 (16)</u> | 0.425 | | | | 13 | 39989.010 | SDR_BCAST_CCC | 0x07 | <u>107-124 (18)</u> | 0.800 | | | |
| 14 | 15491.390 | SDR_BCAST_CCC_TBIT | 0×00 | <u>122-123 (2)</u> | 0.055 | | | ~ | 14 | 39989.810 | SDR_BCAST_CCC_TBIT | 0x00 | <u>125-127 (3)</u> | 0.100 | | | |
| PHY Sta | ates 80-85 | | | | | | | | PHY | States 82-87 | | | | | | | |
| | | | | | | · · · · · · · · | | | | · / [| | | | | | | |
| <u> </u> | 5 | | | L | <u> </u> | | | | e 🗜 | <u>fi</u> | | | | | | | |
| 0 | / | 0.5 <u>1</u> | rel | .5 lative time (u | | 2.5 | 3 | | Ma | | ٥.5 م a repeated start | | lative time (us | | 2.5 | 3 | 3 |
| Fig | ure 91 H | ot-Join FSM | | | Un ri | gnt: ai | tter the | e sia | ves | S HJ LE | equest has | bee | п аск | nowie | eagea | , the ma | as |



• Interoperation example: HDR-DDR

| Go | To: Timesta | mp ~ | Times: | relativeToStart | ~ | | | FSM |
|-------|---------------|--------------------|--------|--------------------|---------------|---------|-----|-----|
| PHY | I3C States | lessages | | | | | | |
| ID | Time (us) | Description | Param | PHY States | Duration (us) | Message | | ^ |
| 21 | 32043.170 | DAA_DADDR | 0x10 | 265-282 (18) | 1.910 | | | |
| 22 | 32045.080 | DAA_DADDR_ACK | 0x00 | <u>283-285 (3)</u> | 0.240 | | | |
| 23 | 32045.320 | DAA_SR | 0x00 | 286-289 (4) | 1.650 | | | |
| 24 | 32046.970 | DAA_I3C_BCAST_RD | 0xFD | 290-306 (17) | 0.810 | | | |
| 25 | 32047.780 | DAA_I3C_BCAST_ACK | 0x01 | <u>307-309 (3)</u> | 0.240 | | | |
| 26 | 32048.020 | DELIM_BUS_IDLE | 0x00 | <u>310-314 (5)</u> | 78696.620 | | | |
| 27 | 110744.640 | SDR_BCAST_I3C_WR | 0xFC | 315-331 (17) | 1.910 | 2 | | |
| 28 | 110746.550 | SDR_BCAST_I3C_ACK | 0x00 | <u>332-333 (2)</u> | 0.240 | | | |
| 29 | 110746.790 | SDR_BCAST_CCC | 0x20 | 334-351 (18) | 0.800 | | | |
| 30 | 110747.590 | SDR_BCAST_CCC_TBIT | 0x00 | <u>352-353 (2)</u> | 0.100 | | | |
| 31 | 110747.690 | DDR_CMD_WORD_PRMB | 0x01 | <u>354-357 (4)</u> | 0.100 | | | |
| 32 | 110747.790 | DDR_CMD_WORD_B0 | 0x00 | 358-365 (8) | 0.400 | | | |
| 33 | 110748.190 | DDR_CMD_WORD_B1 | 0x11 | 366-377 (12) | 0.400 | | | |
| 34 | 110748.590 | DDR_CMD_WORD_PAR | 0x01 | 378-380 (3) | 0.100 | | | |
| 35 | 110748.690 | DDR_WR_DATA_PRMB | 0x03 | 381-392 (12) | | | | |
| PHY S | tates 381-392 | | | | | | | |
| | | | , , | 1 · 1 | • 1 | | | |
| ĥ | 0.2 | 0.4 0.6 0 | 1.8 | 1 12 | 1.4 | 1.6 | 1.8 | 2 |



| • | Interoperat | Go To | o: Timesta | 3C States, 3 Messages mp ~ | Times: | relativeToStart | ~ | | | FSM |
|---|--|--------|-------------------|-------------------------------|------------|-----------------------|---------------|---------|-------|-------|
| | meroperat | ID | Time (us) | Description | Param | PHY States | Duration (us) | Message | | ^ |
| | | 21 | 32043.170 | DAA DADDR | 0x10 | 265-282 (18) | 1.910 | Meaauge | | |
| | | 22 | 32045.080 | DAA_DADDR_ACK | 0x00 | 283-285 (3) | 0.240 | | | |
| | | 23 | 32045.320 | DAA SR | 0x00 | 286-289 (4) | 1.650 | | | |
| | | 24 | 32046.970 | DAA_I3C_BCAST_RD | 0xFD | | 0.810 | | | |
| | | 25 | 32047.780 | DAA_I3C_BCAST_ACK | 0x01 | 307-309 (3) | 0.240 | | | |
| | | 26 | 32048.020 | DELIM_BUS_IDLE | 0x00 | 310-314 (5) | 78696.620 | | | |
| | | 27 | 110744.640 | SDR_BCAST_I3C_WR | 0xFC | 315-331 (17) | 1.910 | 2 | | |
| | | 28 | 110746.550 | SDR_BCAST_I3C_ACK | 0x00 | <u>332-333 (2)</u> | 0.240 | | | |
| | | 29 | 110746.790 | SDR_BCAST_CCC | 0x20 | <u>334-351 (18)</u> | 0.800 | | | |
| | | 30 | 110747.590 | SDR_BCAST_CCC_TBIT | 0x00 | <u>352-353 (2)</u> | 0.100 | | | |
| | | 31 | 110747.690 | DDR_CMD_WORD_PRMB | 0x01 | <u>354-357 (4)</u> | 0.100 | | | |
| | | 32 | 110747.790 | DDR_CMD_WORD_B0 | 0x00 | <u>358-365 (8)</u> | 0.400 | | | |
| | | 33 | 110748.190 | DDR_CMD_WORD_B1 | 0x11 | 366-377 (12) | 0.400 | | | |
| | | 34 | 110748.590 | DDR_CMD_WORD_PAR | 0x01 | <u>378-380 (3)</u> | 0.100 | | | |
| | | 35 | 110748.690 | DDR_WR_DATA_PRMB | 0x03 | <u>381-392 (12)</u> | | | | × |
| | | PHY St | ates 381-392 | | | | | | | |
| | Linguagesefu | | | | ı , | | | | - i · | · · · |
| | - Unsuccessiu | | | | | | | | | |
| | UnsuccessfuUnderlying i | NAC | 0.2 K from the | | .s relativ | 1 1.2 ve time (us) | 1.4 | 1.6 | 1.8 | 2 |



• Interoperation example: HDR-DDR

| | | 3C States, 3 Messages | _ | relativeToStart | ~ | 459 PH Go To | | and tamp | Times: | relativeToStar | t v | | FSM |
|-------|-----------------------------|-----------------------|--------|---------------------|---------------|-----------------|-------------|--------------------|--------|---------------------|---------------|----------|-----------|
| Go | To: Timesta I3C States I | | Times: | relative rootan | ~ | | | Messages | Times: | leiduve robiai | | | 1.3M |
| ID | Time (us) | Description | Param | PHY States | Duration (us) | ID | Time (us) | Description | Param | PHY States | Duration (us) | Message | ^ |
| 21 | 32043.170 | DAA_DADDR | 0x10 | 265-282 (18) | 1.910 | 27 | 96206.770 | SDR_BCAST_I3C_WR | 0xFC | 319-335 (17) | 1.910 | 2 | |
| 22 | 32045.080 | DAA_DADDR_ACK | 0×00 | 283-285 (3) | 0.240 | 28 | 96208.680 | SDR_BCAST_I3C_ACK | 0x00 | 336-337 (2) | 0.240 | | |
| 23 | 32045.320 | DAA_SR | 0×00 | 286-289 (4) | 1.650 | 29 | 96208.920 | SDR_BCAST_CCC | 0x20 | 338-355 (18) | 0.800 | | |
| 24 | 32046.970 | DAA_I3C_BCAST_RD | 0xFD | 290-306 (17) | 0.810 | 30 | 96209.720 | SDR_BCAST_CCC_TBIT | 0×00 | 356-357 (2) | 0.100 | | |
| 25 | 32047.780 | DAA_I3C_BCAST_ACK | 0x01 | <u>307-309 (3)</u> | 0.240 | 31 | 96209.820 | DDR_CMD_WORD_PRMB | 0x01 | <u>358-361 (4)</u> | 0.100 | | |
| 26 | 32048.020 | DELIM_BUS_IDLE | 0x00 | <u>310-314 (5)</u> | 78696.620 | 32 | 96209.920 | DDR_CMD_WORD_B0 | 0x00 | <u>362-369 (8)</u> | 0.400 | | |
| 27 | 110744.640 | SDR_BCAST_I3C_WR | 0xFC | 315-331 (17) | 1.910 | 33 | 96210.320 | DDR_CMD_WORD_B1 | 0x11 | 370-381 (12) | 0.400 | | |
| 28 | 110746.550 | SDR_BCAST_I3C_ACK | 0x00 | <u>332-333 (2)</u> | 0.240 | 34 | 96210.720 | DDR_CMD_WORD_PAR | 0x01 | 382-384 (3) | 0.100 | | |
| 29 | 110746.790 | SDR_BCAST_CCC | 0x20 | 334-351 (18) | 0.800 | 35 | 96210.820 | DDR_WR_DATA_PRMB | 0x02 | <u>385-388 (4)</u> | 0.110 | | |
| 30 | 110747.590 | SDR_BCAST_CCC_TBIT | 0x00 | <u>352-353 (2)</u> | 0.100 | 36 | 96210.930 | DDR_WR_DATA_B0 | 0xFF | <u>389-396 (8)</u> | 0.400 | | |
| 31 | 110747.690 | DDR_CMD_WORD_PRMB | 0x01 | <u>354-357 (4)</u> | 0.100 | 37 | 96211.330 | DDR_WR_DATA_B1 | 0x21 | <u>397-404 (8)</u> | 0.400 | | |
| 32 | 110747.790 | DDR_CMD_WORD_B0 | 0x00 | 358-365 (8) | 0.400 | 38 | 96211.730 | DDR_WR_DATA_PAR | 0x02 | 405-406 (2) | 0.100 | | |
| 33 | 110748.190 | DDR_CMD_WORD_B1 | 0x11 | 366-377 (12) | 0.400 | 39 | 96211.830 | DDR_WR_DATA_PRMB | 0x03 | 407-408 (2) | 0.100 | | |
| 34 | 110748.590 | DDR_CMD_WORD_PAR | 0x01 | <u>378-380 (3)</u> | 0.100 | 40 | 96211.930 | DDR_WR_DATA_B0 | 0x63 | <u>409-416 (8)</u> | 0.400 | | |
| 35 | 110748.690 | DDR_WR_DATA_PRMB | 0x03 | <u>381-392 (12)</u> | | 41 | 96212.330 | DDR_WR_DATA_B1 | 0xB1 | <u>417-426 (10)</u> | 0.400 | | ~ |
| PHY S | States 381-392 | 1 | | | | PHY Sta | ates 362-38 | 8 | | | | | |
| ſ | | | ı . | | · · · | | ····· | | | | | | |
| 15 | 0.2 | 0.4 0.6 (| 0.8 | 1 1.2 | 1.4 | 0 | 0.1 | 0.2 0.3 | 0.4 | | 0.6 0 | .7 0.8 | 0.9 |
| NAG | CK from the | slave | relat | ve time (us) | | | | | rela | tive time (us) | | ACK from | the slave |

- On left: unsuccessful DDR write: the slave issues a NACK
- On right: successful DDR write: the master receives an ACK from slave



• Interoperation example: HDR-DDR

| 22 32045.000 DAA_DADDR_ACK 0x00 283.285.01 0.240 Image: Constraint of the state of the s | ID Time link Description Param PHY States Duration (us) Message 21 32043.170 DAA_DADDR 0x10 265-282.118 1.910 | Go T | To: Timesta | mp ~ | Times: | relativeToStart | ~ | | | FSM |
|---|---|--------------|--------------|--------------------|--------|--------------------|---------------|---------|-----|-----|
| 21 32043.170 DAA_DADDR 0x10 255-282.118 1.910 1.910 22 32045.00 DAA_DADDR_ACK 0x00 283-285.01 0.240 1.650 23 32045.320 DAA_SR 0x00 286-283.61 1.650 1.650 24 32045.920 DAA_SR 0x00 286-283.61 1.650 1.650 24 32045.920 DAA_SR_DEAST_RD 0x10 296-283.61 1.650 1.650 25 32047.720 DAA_J3C_BCAST_RD 0x10 307.309.01 0.240 1.650 26 32048.020 DELIM_BUS_IDLE 0x00 316.314.151 78696.620 1.0104 1.0104 2 21 11074.650 SDR_BCAST_IGZ_CKK 0x00 312.333.61 1.900 2 1.0104 1.0104 1.0104 1.0104 1.0104 1.0104 1.0104 1.0104 1.0104 1.0104 1.0104 1.0104 1.0104 1.0104 1.0104 1.0104 1.0104 1.0107.750 DR_CMD_WORD_B0 | 21 32043 170 DAA_DADDR 0x10 255:282 (18) 1.910 22 32045 320 DAA_SR 0x00 283:285 (3) 0.240 23 32045 320 DAA_SR 0x00 285:282 (4) 1.550 24 32046 320 DAA_ISC_GCAST_RD 0xFD 290:306 (17) 0.310 24 32046 970 DAA_ISC_GCAST_RD 0xFD 290:306 (17) 0.310 25 32047700 DAA_ISC_GCAST_RD 0xFD 290:306 (17) 0.310 26 32048 020 DELIM_BUS_IDLE 0x00 310:314 (5) 78696 620 27 11074 464 SDR_BCAST_I3C_WR 0xFC 315:331 (17) 1910 2 28 11074 590 SDR_BCAST_ICCC 0x00 32:333 (2) 0:400 30 11074 590 SDR_BCAST_ICCC 1600 35:351 (2) 0:100 31 11074 7590 SDR_BCAST_ICCC 100 35:353 (2) 0:100 31 11074 7590 DDR_CMD_WORD_RHMB 0x01 35:351 (2) | РНҮ | I3C States N | Nessages | | | | | | |
| 22 32045.080 DAA_DADDR_ACK 0x00 283.285.03 0.240 Image: Constraint of the state of the s | 22 32045 080 DAA_DADDR_ACK 0x00 283-285 0.3 0.240 Image: Constraint of the constraint | ID | Time (us) | Description | Param | PHY States | Duration (us) | Message | | ^ |
| 23 32045320 DAA_SR 0x00 28528540 1650 24 32046370 DAA_J3C_BCAST_RD 0xFD 290.305.117 0.810 25 32047.780 DAA_J3C_BCAST_RD 0xFD 290.305.117 0.810 26 32048.020 DELIM_BUS_DLE 0x01 307.309.01 0.240 27 10744.400 SDR_BCAST_J3C_WR 0xFC 315.331.117 1910 2 28 110746.550 SDR_BCAST_J3C_ACK 0x00 332.333.621 0.40 29 110747.590 SDR_BCAST_COC 0x00 352.353.621 0.100 21 110747.590 SDR_BCAST_COC 0x00 352.353.621 0.100 21 110747.590 SDR_BCAST_COC 0x00 352.353.621 0.100 21 110747.750 SDR_BCAST_COC 0x00 352.353.621 0.400 21 110747.750 DDR_CMD_PRMB 0x01 352.357.210 0.400 <td>2 32045 320 DAA_SR 0x00 2622232 40 1.850 24 32046 970 DAA_I3C_BCAST_RD 0xFD 293306 177 0.810 25 32047 780 DAA_I3C_BCAST_RD 0xFD 293306 177 0.810 26 32048 020 DELIM_BUS_IDLE 0x00 310314 (2) 78966 620 27 110744 640 SDR_BCAST_J3C_WR 0xFC 315331 (12) 1910 2 28 110746 550 SDR_BCAST_J3C_WR 0xFC 315331 (12) 0.800 29 110746 550 SDR_BCAST_JCCC 0x20 3243351 (18) 0.800 29 110745 590 SDR_BCAST_JCCC_TBIT 0x00 352353 (2) 0.100 31 110747 590 DDR_CMD_WORD_PRMB 0x01 35457 (12) 0.400 32 110747 590 DDR_CMD_WORD_BB 0x11 365457 (12) 0.400 31 110747 590 DDR_CMD_WORD_BB 0x11 3555 (8) 0.400 <!--</td--><td>21</td><td>32043.170</td><td>DAA_DADDR</td><td>0x10</td><td>265-282 (18)</td><td>1.910</td><td></td><td></td><td></td></td> | 2 32045 320 DAA_SR 0x00 2622232 40 1.850 24 32046 970 DAA_I3C_BCAST_RD 0xFD 293306 177 0.810 25 32047 780 DAA_I3C_BCAST_RD 0xFD 293306 177 0.810 26 32048 020 DELIM_BUS_IDLE 0x00 310314 (2) 78966 620 27 110744 640 SDR_BCAST_J3C_WR 0xFC 315331 (12) 1910 2 28 110746 550 SDR_BCAST_J3C_WR 0xFC 315331 (12) 0.800 29 110746 550 SDR_BCAST_JCCC 0x20 3243351 (18) 0.800 29 110745 590 SDR_BCAST_JCCC_TBIT 0x00 352353 (2) 0.100 31 110747 590 DDR_CMD_WORD_PRMB 0x01 35457 (12) 0.400 32 110747 590 DDR_CMD_WORD_BB 0x11 365457 (12) 0.400 31 110747 590 DDR_CMD_WORD_BB 0x11 3555 (8) 0.400 </td <td>21</td> <td>32043.170</td> <td>DAA_DADDR</td> <td>0x10</td> <td>265-282 (18)</td> <td>1.910</td> <td></td> <td></td> <td></td> | 21 | 32043.170 | DAA_DADDR | 0x10 | 265-282 (18) | 1.910 | | | |
| Z4 32046.970 DAA_I3C_BCAST_RD 0xFD 250.306.177 0.810 25 32047.780 DAA_J3C_BCAST_ACK 0x01 307.309.03 0.240 26 32048.020 DELIM_BUS_IDLE 0x00 310.314.67 78696.620 27 110744.640 SDR_BCAST_J3C_WR 0xFC 315.331.117 1910 2 28 110746.550 SDR_BCAST_J3C_WR 0xFC 312.334.67 0x60 29 110746.550 SDR_BCAST_JCCCT 0x00 322.333.47 0x00 30 110747.90 SDR_BCAST_CCCT 0x00 322.333.47 0x100 21 110747.750 SDR_BCAST_CCCT 0x00 322.333.47 0x100 31 110747.90 DDR_CMD_PRMB 0x01 325.353.40 0x100 31 110747.790 DDR_CMD_WORD_PRMB 0x01 325.357.01 0x100 33 110748.190 DDR_CMD_WORD_BB 0x11 326.357.712 0x100 | Z4 32046 970 DAA_I3C_BCAST_RD 0xFD 280302-10 0.810 25 32047 780 DAA_I3C_BCAST_RD 0xFD 280302-10 0.240 26 32048 020 DELIM_BUS_IDLE 0x00 310314 (5) 78596 520 27 110744 640 SDR_BCAST_JCC_WR 0x700 315331 (12) 1310 2 28 110746 550 SDR_BCAST_JCC_WR 0x00 325333 (2) 0.240 2 29 110746 550 SDR_BCAST_JCCC 0x20 324351 (18) 0.800 2 30 110747 590 SDR_BCAST_CCC_TBIT 0x00 352353 (2) 0.100 2 31 110747 590 DDR_CMD_WORD_PRMB 0x01 354357 (12) 0.400 32 32 110747 590 DDR_CMD_WORD_B 0x01 358357 (12) 0.400 33 31 31 110748 190 DDR_CMD_WORD_B 0x11 358357 (12) 0.400 34 110748 590 DDR_CMD_WORD_PAR 0x01 378390 (2) 0.100 34 | 22 | 32045.080 | DAA_DADDR_ACK | 0x00 | 283-285 (3) | 0.240 | | | |
| ZS 32047.780 DAA_ISC_BCAST_ACK 0.01 307.309 0.240 26 32048.020 DELIM_BUS_IDLE 0.00 310.314.60 78696.620 27 110744.640 SDR_BCAST_I3C_WR 0.FC 315.331.117 1910 2 28 110746.550 SDR_BCAST_I3C_ACK 0.00 322.333.02 0.240 29 110746.780 SDR_BCAST_CCC 0.20 334.351.102 0.800 30 110747.780 SDR_BCAST_CCC_TBIT 0.00 352.353.22 0.100 31 110747.780 DDR_CMD_WORD_PRIB 0.01 358.355.60 0.400 31 110747.890 DDR_CMD_WORD_BBI 0.11 265.377.112 0.400 | 25 32047.780 DAA.]35_BCAST_ACK 0x01 307.309 0.240 26 32048.020 DELIM_BUS_IDLE 0x00 310.314.05 78696.620 27 110744.640 SDR_BCAST_J3C_WR 0xFC 315.331.172 1910 2 28 11074.640 SDR_BCAST_J3C_WR 0xFC 315.331.172 1910 2 29 11074.657.05 SDR_BCAST_J3C_WR 0xFC 315.331.172 1910 2 20 11074.6730 SDR_BCAST_JCC_C 0x00 324.351.180 0800 30 11074.790 SDR_BCAST_CCC_TBIT 0x00 354.357.40 0.100 31 11074.790 DDR_CMD_WORD_PRMB 0x01 358.351.00 0.400 32 11074.790 DDR_CMD_WORD_B 0x01 358.357.02 0.400 31 11074.790 DDR_CMD_WORD_PAR 0x01 378.280.02 0.100 34 11074.8590 DDR_CMD_WORD_PAR 0x01 378.280.02 | 23 | 32045.320 | DAA_SR | 0x00 | 286-289 (4) | 1.650 | | | |
| 26 32048.020 DELIM,BUS_IDLE 0.00 310.314_f5 78696.620 27 110744.640 SDR_BCAST_I3C_WR 0xFC 315.331_f17 1.910 2 28 110746.550 SDR_BCAST_I3C_ACK 0x00 322.333_f2 0.240 29 110746.550 SDR_BCAST_CCC 0x20 334.351_f18 0.800 30 110747.590 SDR_BCAST_CCC_TBIT 0x00 352.353_f2 0.100 31 110747.590 DDR_CMD_WORD_PRMB 0x01 354.355_f8 0x00 32 110747.590 DDR_CMD_WORD_B0 0x00 358.356_f8 0400 33 110747.590 DDR_CMD_WORD_B1 0x11 365.377_f12 0400 | 26 32048 020 DELIM_BUS_IDLE 0x00 310-314 (5) 78596 620 27 110744 640 SDR_BCAST_J3C_WR 0xFC 315-331 (17) 1910 2 28 110746 550 SDR_BCAST_J3C_WR 0xFC 315-331 (17) 1910 2 28 110746 550 SDR_BCAST_J3C_WC 0xCO 324-331 (17) 0.040 32 29 110747 590 SDR_BCAST_CCC 0x00 324-351 (18) 0.800 33 31 110747 590 DR_CMD_WORD_PRMB 0x01 352-353 (2) 0.100 32 31 110747 590 DR_CMD_WORD_PRMB 0x01 358-356 (8) 0.400 33 31 110748 190 DR_CMD_WORD_B1 0x11 358-357 (12) 0.400 34 110748 590 DDR_CMD_WORD_PAR 0x01 378-380 (2) 0.100 34 110748 590 DDR_CMD_WORD_PAR 0x01 378-380 (2) 0.100 35 110-32 (12) 400 34 110748 590 DDR_MU_WR_DATA_PRMB 0x03 3113-32 (12) 54 <td>24</td> <td>32046.970</td> <td>DAA_I3C_BCAST_RD</td> <td>0xFD</td> <td>290-306 (17)</td> <td>0.810</td> <td></td> <td></td> <td></td> | 24 | 32046.970 | DAA_I3C_BCAST_RD | 0xFD | 290-306 (17) | 0.810 | | | |
| Z 110744.94 SDR_BCAST_J3C_WR 0.4C 315.33.1.17 1.910 2 28 110746.50 SDR_BCAST_J3C_ACK 0.40 332.333.02 0.40 29 110746.50 SDR_BCAST_J3C_ACK 0.40 332.333.02 0.40 30 110747.590 SDR_BCAST_CCC_TBIT 0.00 352.353.72 0.100 31 110747.590 DDR_CMD_VPRMB 0.00 352.353.72 0.100 31 110747.590 DDR_CMD_WORD_PRMB 0.00 352.357.24 0.100 33 110747.590 DDR_CMD_WORD_B1 0.00 352.357.24 0.100 | Z1 110744.640 SDR_BCAST_J3C_WR ArC 315331.173 1910 2 28 110746.550 SDR_BCAST_J3C_ACK 0x00 332.333.12 0.240 29 110746.550 SDR_BCAST_J3C_ACK 0x00 332.333.12 0.240 30 110746.570 SDR_BCAST_CCC_TBIT 0x00 325.353.117 0.100 31 110747.590 DDR_CMD_WORD_PRIMB 0x10 254.357.40 0.100 31 110747.590 DDR_CMD_WORD_BRI 0x00 355.88 0.400 31 110748.190 DDR_CMD_WORD_BRI 0x11 365.377.112 0.400 33 110748.190 DDR_CMD_WORD_PAR 0x01 378-380.19 0.100 34 110748.190 DDR_CMD_WORD_PAR 0x03 313.132.172 | 25 | 32047.780 | DAA_I3C_BCAST_ACK | 0x01 | <u>307-309 (3)</u> | 0.240 | | | |
| 28 110746.550 SDR_BCAST_I3C_ACK 0x00 332.333_02 0.240 29 110746.570 SDR_BCAST_GCC 0x00 334.351_118 0.800 30 110747.580 SDR_BCAST_CCC_TBIT 0x00 352.353_02 0.100 31 110747.580 DDR_CMD_PRMB 0x01 352.353_02 0.100 21 110747.750 DDR_CMD_WORD_PRMB 0x00 352.355_00 0.400 33 110748.190 DDR_CMD_WORD_B1 0x11 365.377_112 0.400 | 28 110745.550 SDR_BCAST_J3C_ACK 0x00 332,333,22 0.240 29 110745.550 SDR_BCAST_J3C_ACK 0x00 332,333,22 0.240 29 110745.550 SDR_BCAST_J3C_ACK 0x00 332,333,22 0.240 30 110747.590 SDR_BCAST_CCC_TBIT 0x00 352,353,22 0.100 31 110747.590 DDR_CMD_WORD_PRMB 0x01 354,357,40 0.400 32 110747.590 DDR_CMD_WORD_B0 0x00 258,355,40 0.400 31 110747.590 DDR_CMD_WORD_B1 0x11 356,577,172 0.400 34 110748.590 DDR_CMD_WORD_PAR 0x01 278,380,63 0.100 34 110748.590 DDR_CMD_WORD_PAR 0x03 311,312,12 V | 26 | 32048.020 | DELIM_BUS_IDLE | 0x00 | 310-314 (5) | 78696.620 | | | |
| 29 110746.790 SDR_BCAST_CCC 0x20 334.351 (18) 0.800 30 110747.590 SDR_BCAST_CCC_TBIT 0x00 352.353 (2) 0.100 31 110747.590 DDR_CMD_WORD_PRMB 0x01 354.357 (4) 0.100 32 110747.590 DDR_CMD_WORD_B0 0x00 359.365 (8) 0.400 33 110748.190 DDR_CMD_WORD_B1 0x11 266.377 (12) 0.400 | 29 110746.790 SDR_BCAST_CCC 0x20 334.351 (18) 0.800 30 110747.590 SDR_BCAST_CCC_TBIT 0x00 352.353 (2) 0.100 31 110747.590 DDR_CMD_WORD_PRMB 0x01 354.357 (4) 0.100 32 110747.590 DDR_CMD_WORD_BB 0x01 354.357 (12) 0.400 33 110748.190 DDR_CMD_WORD_PAR 0x01 378.380 (2) 0.100 34 110748.590 DDR_CMD_WORD_PAR 0x01 378.380 (2) 0.100 35 110748.690 DDR_K_RDATA_PRMB 0x03 311.322 (12) V | 27 | 110744.640 | SDR_BCAST_I3C_WR | 0xFC | 315-331 (17) | 1.910 | 2 | | |
| 30 110747.590 SDR_BCAST_CCC_TBIT 0x00 352.353.20 0.100 31 110747.590 DDR_CMD_WORD_PRMB 0x01 354.357.40 0.100 32 110747.790 DDR_CMD_WORD_PRMB 0x00 359.365.60 0.400 33 110748.190 DDR_CMD_WORD_B1 0x11 266.377.112 0.400 | 30 110747.590 SDR_BCAST_CCC_TBIT 0x00 352,353.12 0.100 31 110747.590 DDR_CMD_WORD_PRMB 0x01 354,357.14 0.100 32 110747.590 DDR_CMD_WORD_PRMB 0x01 354,357.14 0.100 33 110748.190 DDR_CMD_WORD_B1 0x11 356,357.12 0.400 34 110748.590 DDR_CMD_WORD_PAR 0x01 378,380.03 0.100 35 110748.690 DDR_LMD_WORD_PAR 0x03 311,322.12 V | 28 | 110746.550 | SDR_BCAST_I3C_ACK | 0x00 | <u>332-333 (2)</u> | 0.240 | | | |
| 31 110747.890 DDR_CMD_WORD_PRMB 0x01 354.357.01 0.100 32 110747.790 DDR_CMD_WORD_B0 0x00 358.365.60 0.400 33 110748.190 DDR_CMD_WORD_B1 0x11 265.377.012 0.400 | 31 110747.690 DDR_CMD_WORD_PRMB 6x01 354.357.41 0.100 32 110747.790 DDR_CMD_WORD_B0 6x00 358.365.48 0.400 33 110748.190 DDR_CMD_WORD_B1 0x11 256.377.112 0.400 34 110748.590 DDR_CMD_WORD_PAR 6x01 378-380.03 0.100 34 110748.690 DDR_WR_DATA_PRMB 6x03 331392.172 | 29 | 110746.790 | SDR_BCAST_CCC | 0x20 | 334-351 (18) | 0.800 | | | |
| 32 110747.790 DDR_CMD_WORD_B0 0x00 358.355.00 0.400 33 110748.190 DDR_CMD_WORD_B1 0x11 356.377.112 0.400 | 32 110747.790 DDR_CMD_WORD_B0 0x00 328.355.00 0.400 33 110748.190 DDR_CMD_WORD_B1 0x11 366.377.122 0.400 34 110748.590 DDR_CMD_WORD_PAR 0x01 378.380.03 0.100 35 110748.690 DDR_WR_DATA_PRMB 0x03 321.352.12 V | 30 | 110747.590 | SDR_BCAST_CCC_TBIT | 0x00 | <u>352-353 (2)</u> | 0.100 | | | |
| 33 110748.190 DDR_CMD_WORD_B1 0x11 366-377 (12) 0.400 | 33 110748.190 DDR_CMD_WORD_B1 0x11 265-377.122 0.400 34 110748.590 DDR_CMD_WORD_PAR 0x01 278-380.13 0.100 35 110748.690 DOR_WR_DATA_PRMB 0x03 321332.12 | 31 | 110747.690 | DDR_CMD_WORD_PRMB | 0x01 | <u>354-357 (4)</u> | 0.100 | | | |
| | 34 110748.590 DDR_CMD_WORD_PAR 0x01 378.380 0.100 35 110748.690 DDR_WR_DATA_PRMB 0x03 321.332.172 | 32 | 110747.790 | DDR_CMD_WORD_B0 | 0×00 | 358-365 (8) | 0.400 | | | |
| 34 110748.590 DDR CMD WORD PAR 0x01 378-380 (3) 0.100 | 35 110748.690 DDR_WR_DATA_PRMB 0x03 351-392 (12) | 33 | 110748.190 | DDR_CMD_WORD_B1 | 0x11 | 366-377 (12) | 0.400 | | | |
| | | 34 | 110748.590 | DDR_CMD_WORD_PAR | 0x01 | 378-380 (3) | 0.100 | | | |
| 35 110748.690 DDR_WR_DATA_PRMB 0x03 381-392 (12) | PHY States 381-392 | 35 | 110748.690 | DDR_WR_DATA_PRMB | 0x03 | 381-392 (12) | | | | ~ |
| | | \backslash | 1. | | | | | | | . – |
| | | · > | 0.2 | 0.4 0.6 0 | | 1 1.2 | 1.4 | 1.6 | 1.8 | 2 |
| | | NAC | K from the | slave | relat | ive time (us) | | | | |

| ID | | Messages | | | | | |
|----|-----------|--------------------|-------|--------------------|---------------|---------|--|
| | Time (us) | Description | Param | PHY States | Duration (us) | Message | |
| 27 | 96206.770 | SDR_BCAST_I3C_WR | 0xFC | 319-335 (17) | 1.910 | 2 | |
| 28 | 96208.680 | SDR_BCAST_I3C_ACK | 0×00 | <u>336-337 (2)</u> | 0.240 | | |
| 29 | 96208.920 | SDR_BCAST_CCC | 0x20 | 338-355 (18) | 0.800 | | |
| 30 | 96209.720 | SDR_BCAST_CCC_TBIT | 0x00 | <u>356-357 (2)</u> | 0.100 | | |
| 31 | 96209.820 | DDR_CMD_WORD_PRMB | 0x01 | <u>358-361 (4)</u> | 0.100 | | |
| 32 | 96209.920 | DDR_CMD_WORD_B0 | 0x00 | <u>362-369 (8)</u> | 0.400 | | |
| 33 | 96210.320 | DDR_CMD_WORD_B1 | 0x11 | 370-381 (12) | 0.400 | | |
| 34 | 96210.720 | DDR_CMD_WORD_PAR | 0x01 | <u>382-384 (3)</u> | 0.100 | | |
| 35 | 96210.820 | DDR_WR_DATA_PRMB | 0x02 | <u>385-388 (4)</u> | 0.110 | | |
| 36 | 96210.930 | DDR_WR_DATA_B0 | 0xFF | <u>389-396 (8)</u> | 0.400 | | |
| 37 | 96211.330 | DDR_WR_DATA_B1 | 0x21 | <u>397-404 (8)</u> | 0.400 | | |
| 38 | 96211.730 | DDR_WR_DATA_PAR | 0x02 | 405-406 (2) | 0.100 | | |
| 39 | 96211.830 | DDR_WR_DATA_PRMB | 0x03 | 407-408 (2) | 0.100 | | |
| 40 | 96211.930 | DDR_WR_DATA_B0 | 0x63 | 409-416 (8) | 0.400 | | |
| 41 | 96212.330 | DDR_WR_DATA_B1 | 0xB1 | 417-426 (10) | 0.400 | | |

- On left: unsuccessful DDR write: the slave issues a NACK
- On right: successful DDR write: the master receives an ACK from slave



| | tates Messages | | elav T Sta | exar | nple | R- | PHY | I3C States | | Times: | relative To Star | t ~ | | FSM | |
|--------------|----------------------------|--------|---------------------|---------------|---------|----|-------|----------------|--------------------|--------|---------------------------------|---------------|---------|--------------------|---|
| ID Time | e (us) Description | Param | PHY States | Duration (us) | Message | ^ | ID | Time (us) | Description | Param | PHY States | Duration (us) | Message | | ^ |
| 21 3204 | 43.170 DAA_DADDR | 0x10 | 265-282 (18) | 1.910 | | | 27 | 96206.770 | SDR_BCAST_I3C_WR | 0xFC | 319-335 (17) | 1.910 | 2 | | 1 |
| 22 3204 | 45.080 DAA_DADDR_ACK | 0x00 | 283-285 (3) | 0.240 | | | 28 | 96208.680 | SDR_BCAST_I3C_ACK | 0x00 | <u>336-337 (2)</u> | 0.240 | | | |
| 23 3204 | 45.320 DAA_SR | 0x00 | 286-289 (4) | 1.650 | | | 29 | 96208.920 | SDR_BCAST_CCC | 0x20 | 338-355 (18) | 0.800 | | | |
| 24 3204 | 46.970 DAA_I3C_BCAST_RD | 0xFD | 290-306 (17) | 0.810 | | | 30 | 96209.720 | SDR_BCAST_CCC_TBIT | 0x00 | <u>356-357 (2)</u> | 0.100 | | | |
| 25 3204 | 47.780 DAA_I3C_BCAST_ACK | 0x01 | <u>307-309 (3)</u> | 0.240 | | | 31 | 96209.820 | DDR_CMD_WORD_PRMB | 0x01 | <u>358-361 (4)</u> | 0.100 | | | |
| 26 3204 | 48.020 DELIM_BUS_IDLE | 0x00 | <u>310-314 (5)</u> | 78696.620 | | | 32 | 96209.920 | DDR_CMD_WORD_B0 | 0x00 | <u>362-369 (8)</u> | 0.400 | | | |
| 27 1107 | 744.640 SDR_BCAST_I3C_WR | 0xFC | 315-331 (17) | 1.910 | 2 | | 33 | 96210.320 | DDR_CMD_WORD_B1 | 0x11 | 370-381 (12) | 0.400 | | | |
| 28 1107 | 746.550 SDR_BCAST_I3C_ACK | 0x00 | <u>332-333 (2)</u> | 0.240 | | | 34 | 96210.720 | DDR_CMD_WORD_PAR | 0x01 | <u>382-384 (3)</u> | 0.100 | | | |
| 29 1107 | 746.790 SDR_BCAST_CCC | 0x20 | 334-351 (18) | 0.800 | | | 35 | 96210.820 | DDR_WR_DATA_PRMB | 0x02 | <u>385-388 (4)</u> | 0.110 | | | |
| 30 1107 | 747.590 SDR_BCAST_CCC_TBIT | 0x00 | <u>352-353 (2)</u> | 0.100 | | | 36 | 96210.930 | DDR_WR_DATA_B0 | 0xFF | <u>389-396 (8)</u> | 0.400 | | | |
| 31 1107 | 747.690 DDR_CMD_WORD_PRMB | 0x01 | 354-357 (4) | 0.100 | | | 37 | 96211.330 | DDR_WR_DATA_B1 | 0x21 | <u>397-404 (8)</u> | 0.400 | | | |
| 32 1107 | 747.790 DDR_CMD_WORD_B0 | 0x00 | 358-365 (8) | 0.400 | | | 38 | 96211.730 | DDR_WR_DATA_PAR | 0x02 | 405-406 (2) | 0.100 | | | |
| 33 1107 | 748.190 DDR_CMD_WORD_B1 | 0x11 | 366-377 (12) | 0.400 | | | 39 | 96211.830 | DDR_WR_DATA_PRMB | 0x03 | <u>407-408 (2)</u> | 0.100 | | | |
| 34 1107 | 748.590 DDR_CMD_WORD_PAR | 0x01 | 378-380 (3) | 0.100 | | | 40 | 96211.930 | DDR_WR_DATA_B0 | 0x63 | <u>409-416 (8)</u> | 0.400 | | | |
| 35 1107 | 748.690 DDR_WR_DATA_PRMB | 0x03 | <u>381-392 (12)</u> | | | ~ | 41 | 96212.330 | DDR_WR_DATA_B1 | 0xB1 | 417-426 (10) | 0.400 | | | ~ |
| PHY States 3 | 381-392 | ' | | | | | PHY S | itates 362-388 | | | | | | | |
| NACK from | m the slave | relati | ve time (us) | | | | | | a NACK | | 0.5 tive time (us) n slav | / | | 0.9 n the slave | |

Analyzer tools ensure interoperation debug goes smoothly



Conclusions and Best Practices

- MIPI[®] I3C[™] has great potential to provide a fast sensor and control bus, and can save a lot of pins on devices and traces on PCBs
- To help ensure interoperability:
 - First principles for layout
 - Power and ground, designing buses for test, bus capacitance
 - Understand signal timing issues
 - Small adjustments can make a big difference for interoperability
 - Protocol implementation
 - Having analysis tools can help make interoperability debug smooth



ADDITIONAL RESOURCES

- <u>https://www.mipi.org/specifications/i3c-sensor-specification</u>
 - MIPI[®] I3C[™] Specifications
- <u>https://www.mipi.org/sites/default/files/mipi_I3C-and-I3C-Basic_app-note-system-integrator</u>
 - System Integrators Application Note for MIPI[®] I3C[™] v1.0 and I3C[™] Basic v1.0
- <u>https://introspect.ca/</u>
 - Total solutions for most high-speed interface technologies
- <u>https://introspect.ca/products-solutions/i3c-design-and-test/</u>
 - I3C design and test solutions
- <u>https://register.gotowebinar.com/register/8766219688391017985</u>
 - I3C Webinar

mipi[®] DEVCON VIRTUAL EVENT

THANK YOU

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