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MIPI[®] A-PHYSM: Laying the Groundwork for MIPI's Automotive SerDes Solutions

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MIPI ALLIANCE DEVELOPERS CONFERENCE

22-23 SEPTEMBER 2020



Presentation Outline

MIPI A-PHY – System View Ariel Lasry

Director, MIPI Alliance Board of Directors

MIPI A-PHY – Specification Overview Edo Cohen

MIPI A-PHY Subgroup Vice-Lead

Q&A



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MIPI A-PHY – System View Ariel Lasry - MIPI Alliance Board Director MIPI ALLIANCE DEVELOPERS

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Auto Industry Transformation



Honda and GM Partner to Develop Mass Produced, Driverless Cars Source: October 4, 2018, Automotive News

MIPI directly supports CASE via:

- Connected (MIPI RFFESM, others)
- Automated (MIPI A-PHY, MIPI CSI-2SM, others)

CASE:

- Connected Automated
- Shared
 Electrified
 - Connected: The move to 5G
 - Automated: The move to L2/L2+ and beyond
 - Shared: New OEMs, new business models, new alliances
 - Electrified: Tesla and others

And . . .

Safety: Improved government safety regulations (FCWS, AEB, RVS, LDWS, etc.) Fuel economy: Aggressive regulations

RFFE: RF Front End

FCWS: Forward Collision Warning System

LDWS: Lane Departure Warning System

AEB: Autonomous Emergency Breaking

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NCAP Regulations Driving Sensors & Display Adoption



- Worldwide NCAP ADAS and ADS standards driving adoption of multiple high data rate "surround sensors"
- Displays for driver viewing of assistance imaging and information also require

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What is MIPI A-PHY?

- MIPI A-PHY is a physical layer specification targeted for ADAS/ADS surround sensor applications and Infotainment display applications in automotive. Version 1.0 will provide a 15-meter reach and data rates of 2-16 Gbps, with a roadmap to 24, 48 Gbps and beyond.
- MIPI A-PHY is the ONLY standard interface to support native camera (MIPI CSI-2SM) and display (MIPI DSI-2SM)

interfaces for automotive. An adaptation layer is also being developed for VESA DisplayPort and eDP.



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Challenges to be solved require: A-PHY + MIPI Protocols

Camera sensor

Display

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Robust Automotive Long Reach Link	 PER = 10⁻¹⁹: 1 packet error in ~10000 car-lifetimes High Speed Downlink and aggregation to support multiple 4K cameras and displays Asymmetric high speed link with fixed low latency ~6μs @G5
End to End Functional Safety	 Enabling Integration of devices using MIPI protocols over A-PHY in ASIL B or ASIL D Systems A-PHY and Protocols (CSI-2, DSI-2) FuSa from Source to Sink
End to End Security	 Authentication; prevention of tampering (malicious and non-malicious) High Definition Content Protection (HDCP) for display applications
Heterogeneous Interfaces	 Common support for multiple display protocols: DSI, Display Port, eDP, OpenLDI Agnostic to source/sink PHY configuration : C-PHY, D-PHY, Lanes count

• Agnostic to source/sink PHY configuration : C-PHY, D-PHY, Lanes count



MASS: MIPI Automotive SerDes Solutions

A vision for End-to-End System





Automotive Protocol Stack-up Diagram



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MIPI A-PHY – Specification overview Edo Cohen - MIPI A-PHY Subgroup Vice-Lead

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Gears and Profiles

- One Rate/line-code/modulation per Downlink Gear
- Single Uplink Gear
- Two Noise/Performance Profiles (with full inter-profile interoperability):
 - Profile 1: optimized for low cost/power implementations for the lower gears with lower Noise immunity and target PER of <10⁻⁹
 - Profile 2: optimized for Vehicle Life-span, link robustness for all Gears with high noise immunity and target PER of <10⁻¹⁹
- A-PHY Device supporting Gear N (N could be 1–5) shall support all lower gears.

Gear Data Rate	Modulation [One modulation per Gear]	Symbol Rate [GBaud]	Net Application Data Rate [Gbps]
G1 2 Gbps	NRZ-8b/10b	2	1.5
G2 4 Gbps	NRZ-8b/10b	4	3
G3 8 Gbps	PAM4	4	7.2
G4 12 Gbps	PAM8	4	10.8
G5 16 Gbps	PAM16	4	14.4
Uplink, All Gears 100Mbps	NRZ-8b/10b	0.1	0.055 (55Mbps)



Interconnect Channel

- A-PHY is a single lane, point-to-point, serial communication technology
- Support for multiple cable types SDP/Coax
- Power over Cable support
- Up to 15m with 4 inline connectors





High Level Structure

- Native Protocol
 - e.g. MIPI CSI-2, MIPI DSI-2, I2C, GPIO
- Protocol Adaptation Layer (PAL)
 - Mapping to/from Native Protocol to A-Packet
- APPI
 - Interface between A-PHY Port and PAL
- Data Link Layer
 - Performs A-Packet scheduling, prioritization and forwarding
- Physical Layer
 - Encodes and decodes symbols extracted from A-Packets according to the modulation scheme used per Gear.
 - Modulated symbols are transmitted and received over the A-PHY interconnect according to the medium-dependent electrical specifications



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PHY Layer

- Unified structure to reduce complexity
- Shared 8B/10B PCS for G1/G2 and Uplink
- RTS Sub-Layer
 - Manage Data Pacing and buffering
 - Assign Message Counter (MC) and CRC
 - P2 the retransmission process for A-Packets that are erroneous or that are not received
- PCS Sub-Layer
 - specifies the conversion of Data Link Layer A-Packets into PHY Symbols.
 - In P2, PCS also handles the JITC^(*) Re-Training
- PMD Sub-Layer
 - Defines the electrical specifications and the physical medium

(*) JITC – Just In Time Cancelers (Cancellers that are used only when needed as channel changes)



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RTS - Time Bounded Local PHY Level Retransmission

• Time Bounded

- Retransmission is attempted only within predefined "Overall Delay" (e.g. ~6μS @G5)
- Local PHY Level
 - Transparent to upper layers
 - Happens within a single A-PHY Hop
- Dynamically Modulated
 - Retransmitted packets has better error resistant data payload Sub-Constellation.
- Highly Reliable
 - PER (Packet Error Rate) < 10⁻¹⁹
- Highly Resilient
 - Overcome Thousands symbols-long Error bursts
 - Multiple 10s of mVs, instantly attacking, NBI Peak.

Low Overhead

− Overall PHY + Link < 10% → 90% Net Data rate</p>



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Data Link Layer

- The A-PHY Data Link Layer is a protocol agnostic layer that performs scheduling, prioritization and forwarding of A-Packets.
- Each Protocol Adaptation Layer has at least one APPI connection to the A-PHY Data Link Layer.
- A-PHY Data Link Layer may be connected to multiple Protocols Adaptation Layers using a single Local Function.
- The A-PHY Data Link Layer may have a single A-PHY Network Function connected to it, or multiple A-PHY Network Functions



- The A-PHY Data Link Layer Enables A-Packet:
 - Forwarding
 - Prioritization
 - Duplication
 - Scheduling



Functional Safety

- A-PHY packets are end-to-end protected as recommended in ISO-26262:2018:
 - CRC-32 for each packet, providing a Hamming-Distance of more than 3.
 - Message Counter that is 8 bits wide.
 - Timeout monitoring is fulfilled by the Keep-Alive function.
- The above measures are necessary to argue a high diagnostic coverage for a communication bus, per *Table D.6* in ISO 26262-5:2018
- All other functional safety features necessary in order to fulfil the required system-level safety goal with ASIL is expected to be managed by upper layers.



Noise Immunity

- There is a major variance in the OEM EMC requirements, from those who aim for minimal noise immunity, to OEMs that apply stringent requirement to protect their system
- A-PHY two profiles provide two noise immunity levels, to accommodate this variance.
 - P1 has lower noise immunity, similar to other SERDES solutions and is applicable for G1 and G2 (optional G3)
 - P2 has very high noise immunity based on MIPI Alliance analysis of expected noise level for the car life-time period.
- MIPI conducted multiple tests in an independent labs evaluating the noise levels and shielding effect degradation after mechanical stress and aging
 - The results helped evaluate the different available technologies
 - The research continues as part of MIPI A-PHY SG activities



Characteristics of RF Ingress Test

Test Conditions

Cable: Two types of Dynamics Coax cables in length of 2m and 15m

Lab Conditions:





Bending Fatigue & Temperature Cycling Test



Screening Attenuation Test Result



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A-PHY Future Outlook

- MIPI is working on the upcoming MIPI A-PHY V1.1 release
- This is an incremental version to the A-PHY V1.0
- Main A-PHY V1.1 features
 - Up to 32Gbps throughput using Dual Lane Downlink support over STQ cables
 - Double Rate Uplink (DRU) with 125Mbps Uplink effective throughput
 - PAM-4 support for lower gears Better noise immunity with lower working frequency enabling usage of lower costs cables and connectors
- Additional Protocol Adaptation Layers 100Mbps ETH and I2S



Concluding Thoughts

- In-vehicle architecture is **rapidly evolving** . . .
- Increased focus on surround sensor applications for ADAS / autonomous driving . . . Best served by dedicated high-speed asymmetric interfaces from sensors to ECU.
- Standardization important for economies of scale, lower cost & greater capabilities.
- The native MIPI protocols (CSI-2, DSI-2, I3C, others, available in billions of devices) with **A-PHY deliver enormous benefit** to the automotive industry . . . performance, cost, noise immunity, and long-term EBOM reduction via elimination of interface bridges.
- The MIPI solution is being developed to **meet the broadest spectrum** of automotive industry needs . . . with anticipated SOP as early as 2024.

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THANK YOU

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