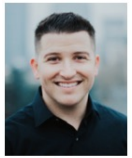
mipi® DEVCON

MIPI ALLIANCE DEVELOPERS CONFERENCE

28-29 SEPTEMBER 2021

Tim McKee, Intel Corporation, MIPI I3C Working Group Chair
Matthew Schnoor, Intel Corporation, MIPI I3C HCI Subgroup Lead
Eyuel Zewdu Teferi, STMicroelectronics, MIPI I3C Basic Ad-hoc Working Group Vice Chair
Radu Pitigoi-Aron, Qualcomm Technologies Inc.
Ian Smith, MIPI Alliance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MIPI I3C Under the Spotlight: A Fireside Chat with the I3C Experts

New Specifications for 2021

- **I3C Version 1.1.1**
  - Clarifications (Small errors and typos)
  - Terminology changes (Controller/Target)
  - Incorporation of previous modifications (Target Reset)
- **I3C Basic Version 1.1.1**
  - Synchronized with I3C v1.1.1
  - Clarifications and Terminology changes
  - New features (HDR Modes, CCCs, Timing Control)
- **I3C Host Controller Interface (HCI) Version 1.1**
  - New features (Grouped Addressing, Dynamic Address Assignment, CCCs with Defining Bytes, Target Reset etc.)
  - Synchronized with I3C v1.1.1 / I3C Basic v1.1.1
  - Clarifications and Terminology changes

Comparison of Features

Feature	I3C v1.0	I3C Basic v1.0	I3C v1.1.1	I3C Basic v1.1.1
12.5 MHz SDR (Controller, Target and Legacy I²C Target Compatibility)	✓	✓	✓	✓
Target can operate as I²C device on I²C bus and on I3C bus using HDR modes	✓	✓	✓	✓
Target Reset	✗	✗	✓	✓
Specified 1.2V-3.3V Operation for 50pf C load	✓	✓	✓	✓
In-Band Interrupt (w/MDB)	✓	✓	✓	✓
Dynamic Address Assignment	✓	✓	✓	✓
Error Detection and Recovery	✓	✓	✓	✓
Secondary Controller	✓	✓	✓	✓
Hot-Join Mechanism	✓	✓	✓	✓
Common Command Codes (Required/Optional)	✓	✓ ✗	✓	✓ ✗
Specified 1.0V Operation for 100pf C load	✗	✓	✗	✓
Set Static Address as Dynamic Address CCC (SETAASA)	✗	✓	✓	✓
Synchronous Timing Control	✓	✗	✓	✗
Asynchronous Timing Control (Mode 0)	✓	✗	✓	✓
Asynchronous Timing Control (Mode 1-3)	✓	✗	✓	✗
HDR-DDR	✓	✗	✓	✓
HDR-TSL/TSP	✓	✗	✓	✗
HDR-BT (Multi-Lane Bulk Transport)	✗	✗	✓	✓
Grouped Addressing	✗	✗	✓	✓
Device to Device(s) Tunneling	✗	✗	✓	✗
Multi-Lane for Speed (Dual/Quad for SDR and HDR-DDR)	✗	✗	✓	✗
Monitoring Device Early Termination	✗	✗	✓	✗

Where is I3C Being Leveraged?

- **JEDEC**
  - Serial Presence Detect (SPD) Hub for DDR Memory
- **DMTF**
  - Management Component Transport Protocol (MCTP) and I3C protocols for bus management
- **Others in development**
  - PCIe I3C sideband
  - I3C over IEEE 1722
  - Protocol Adaptation Layer (PAL) for I3C over A-PHY
  - ETSI for Smart Secure Platform
  - More?

Get Involved / Sources of Further Information

- **I3C Working Group**
  - Open to MIPI contributor members (Meets: Wednesdays 8am PST)
- **Contact the Working Group**
  - Let us know your questions/comments
  - Email: i3c@mipi.org (members)
  - Email: admin@mipi.org (non-members)
- **I3C Supporting Documents**
  - FAQs
  - App Notes
  - Errata
- **Website:** https://www.mipi.org/specifications/i3c-sensor-specification